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A Low Voltage Low Power High Performance FGMOS Based Current Mirror

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Abstract

A high performance FGMOS based current mirrors at low supply voltage is proposed in this paper. A combination of floating gate and CMOS technology is used to design this new simple current mirror at low supply voltage of 0.5V using 180nm CMOS technology. Very low input impedance of 14Ω with increased input voltage swing. In addition to accurate current copy, a very high output impedance of 5GΩ is achieved with low power consumption of 42.6 μW.

Keywords: floating gate MOS, low power, low voltage

1 Introduction

The demand of low voltage low power analog circuits is increasing gradually for portable electronics devices [1]. The speed of analog circuits degrades as supply voltage decreases. It's a challenge to design and develop high performance analog

circuits with minimum power consumption and supply voltage without any compromise in performance. One of the basic analog building blocks is current mirror. A high performance current mirror should have low input impedance and very high output impedance at low supply voltage with accurate current transfer. The input and output voltage requirements should be low and it should be able to operate at high frequency. Various high performance CMOS current mirrors have been introduced with low supply voltage, input impedance and good current copy property [2-11]. Current mirror is used in various applications in analog integrated circuits such as operational amplifiers, current conveyors, operational transconductance amplifiers, analog-to-digital and digital-to-analog data converters, current sensing circuits, current-mode filters, and translinear loops [5–10]. Current mirrors are basically used for current amplification, level shifting, biasing, and loading in a circuit. A current mirror should have very low input impedance and very high output impedance. Shunt feedback technique and flipped voltage follower can be used to achieve very low input impedance [15]. Several output stages have also been proposed to provide high output impedance [12-14] for CMOS current mirrors. The structures proposed in [12-13] are complex implementation of regulated cascode structure and super cascode structure is implemented in [13]. The cascoding of transistor upgrades the output impedance but also increases supply voltage requirements. Many topologies [15-18] have been proposed to implement low input impedance using shunt feedback and a flipped voltage follower in input section .Series feedback is also used in the output section ensuring low input and output impedances but again with high supply voltage requirements.

Floating gate technology provides solution to this problem as it reduces supply voltage requirements and power dissipation of a system. FGMOS based circuits can operate below the limits of supply voltage levels with any affecting the other features of the system with less power dissipation compared to conventional system of same technology [16-18].

In this paper both floating gate technology and cascoding are utilized to propose a new output stage for current mirrors. This paper is organized as follows. Section 2 illustrates the characteristics of floating gate MOSFET. Section 3 covers the implementation of proposed low voltage current mirror and Section 4 depicts small signal analysis of the input and output impedance. The simulation results of both output stages are compared in section 5 and conclusion is given in section 6.

2 Floating Gate MOSFET

Floating gate MOSFET is a multiple input transistor with its floating gate in terms of DC operating point, formed by polysilicon layer and secondary gates are formed above floating gate by other polysilicon layer. A possible equivalent structure of multiple-input FGMOS is given in fig. 1 with symbol and voltage definitions.

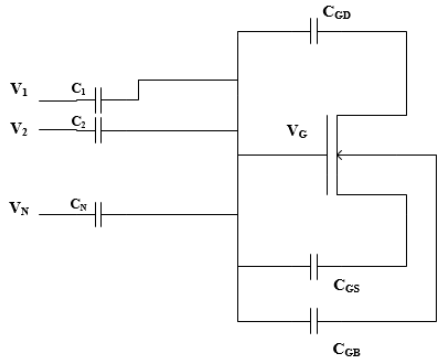


Figure 1: Symbol of floating gate MOSFET.

FGMOS's capacitance can be represented, fig. 1 as set of input capacitors C_i where i= [1,N] between floating gate and inputs as well as parasitic capacitors present in MOSFET[16]. The total capacitance can be given represented as equation 1. V_{FG} is floating gate voltage and can be represented as mentioned in equation 2 under the assumption that floating gate is perfectly isolated where V_i are the inputs voltages and QFG is amount of charge trapped during fabrication process in floating gate.

$$\mathrm{CT} = \mathrm{CGD} + \mathrm{CGS} + \mathrm{CGB} + \sum_{i=1}^{N} Ci \tag{1}$$

$$\mathrm{VFG} = \sum_{i=1}^{N} \frac{\mathrm{Ci}}{\mathrm{CT}} + \frac{\mathrm{CGSVS}}{\mathrm{CT}} + \frac{\mathrm{CGSVD}}{\mathrm{CT}} + \frac{\mathrm{QFG}}{\mathrm{CT}} \tag{2}$$

I_D, the drain current of FGMOS in saturation region can be given as equation 3

$$\mathrm{ID} = \frac{\mu \mathrm{CoxW}}{2\mathrm{L}} \left(\sum_{\mathrm{i}=1}^{\mathrm{N}} \frac{\mathrm{CiViS}}{\mathrm{CT}} + \frac{\mathrm{CGDVDS}}{\mathrm{CT}} + \frac{\mathrm{CGBVBS}}{\mathrm{CT}} + \frac{\mathrm{QFG}}{\mathrm{CT}} - \mathrm{VT}\right)^2 \tag{3}$$

Where W is width and L is length of FGMOS, V_T is threshold voltage, V_S,V_D,V_B denotes voltages at source, drain and bulk terminals.
For two input FGMOS, the current equation can be given as

$$\mathrm{ID} = \frac{\beta}{2}\left(\left(\frac{\mathrm{C1VB+C2Vi}}{\mathrm{CT}}\right) - \mathrm{VT}\right)^2 \tag{4}$$

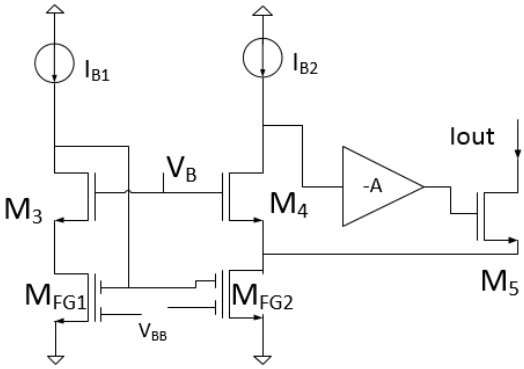
Where β is transconductance parameter and Vi is input voltage.

3 Proposed Current Mirror

Several input and output stages have been proposed for low voltage CMOS current mirrors to achieve high performance. In this proposed current mirror, a flipped voltage follower [18] is used for input stage with mirror transistors implemented using FGMOS transistors and output stage is implemented by super cascade structure [14] as shown in the figure 2.In the input stage shown in figure 2, M_{FG1} and M_{FG2} are FGMOS transistors which are independent of threshold voltage. M3 along with I_B and V_B controls and forces the V_{DS} of FGMOS transistor M_{FG1} to

a constant value. The power supply required by current mirror is limited by input section i.e by transistor M_{FG1}, M3 operating in saturation region and biasing current. The minimum voltage supply required can be given as
$V_{DDminimum} = V_{DSAT} + V_{GS}/k(5)$

Where V_{DSAT} is saturation voltage, V_{GS} is gate to source voltage and k is capacitive voltage divider ratio.



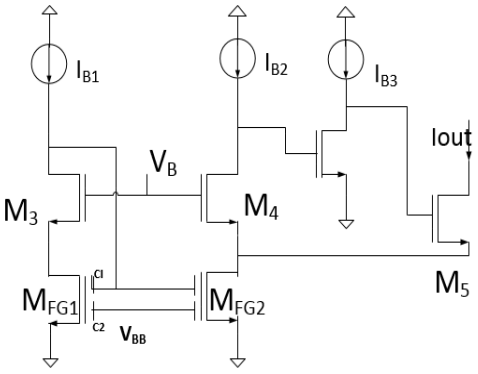


Figure 2: Proposed low voltage current mirror. Figure 3: Proposed low voltage current mirror with inverting amplifier implementation.

It can be seen that minimum supply voltage has been reduced by one V_{DSAT} when compared to voltage requirements if mirror transistors were implemented by CMOS M1 and M2.On the output side, transistor M4 controls and forces the V_{DS} of transistor M2 to be equal to M1. As shown in the fig 2. The drain terminal of transistor M4 is driving the gate of transistor M5 which is in reverse polarity. So, an inverting stage is added to change the polarity while driving gate of transistor M5 along with gain boosting which will increase the output Impedance. A simple realization of inverting stage is shown in the fig. 3.An inverting amplifier formed using a biasing current and transistor M6. The arrangement of transistor M4, M5and M6 along with their biasing currents I_B and I_{B1}forms super cascode structure.

4 Small Signal Analysis

I. Input Impedance

The input impedance, r_{in} is very low due to the presence of input feedback and $M_{FG1.}$ The small signal model of input section is given in fig. 4.

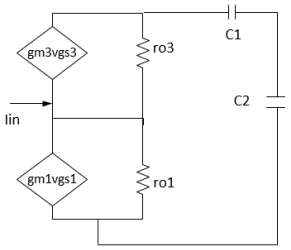


Figure 4: Small signal model for input section

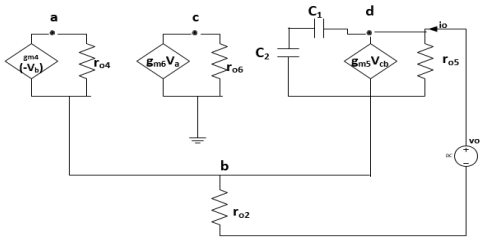


Figure 5: Small signal model of output section

vfg1 can be given as

$$vfg1 = vd3 * \frac{C1}{C1+C2} = k * vd3 \quad (6)$$

$$k = \frac{C1}{C1+C2} \quad (7)$$

Therefore, the small signal trans conductance of M_{FG1}can be given as

$$gmf1 = gm1 * \frac{C1}{CT} \quad (8)$$

where gm is small signal transconductance of NMOS transistor and CT is the total capacitance given by equation (1)
Hence, the input impedance can be given as

$$rin = \frac{1}{kgm1gm3ro3} \quad (9)$$

which is further reduced by the factor k depending upon the values of C1 and C2 connected to two input FGMOS transistor.

II. Output Impedance

The output section is consists of MOSFETs M_{FG2}, M_4, M_6 and M_5 and its equation can be derived from small signal model shown in the fig. 5
r_{out} can be given as

$$rout = \frac{vo}{io} \quad (10)$$

Using equations (1) and (2), the output current can be given as

$$io = gm5vcb\ \frac{CT}{C1} * \frac{vo-vb}{ro5} \quad (11)$$

where

$$vb = io * ro2$$

$$vc = -gm6va * ro6$$

$$va - vb = gm4va * ro4$$

After simplifying, i_o can be calculated as

$$\frac{vo}{ro5} = io\left(1 + \left(gm5gm6ro6(1 + gm4ro4) + gm5 + \frac{1}{ro5}\right) ro2\right) \quad (12)$$

Assuming that $g_m r_o >> 1$, equation (12) can be rewritten as

$$\frac{vo}{io} = rout = gm4ro4gm5ro5gm6ro6ro2 \quad (13)$$

It can be observed form above equation that output impedance is quite high using super cascade structure [13].

5 Simulation Results

The circuit shown in the fig. 6 is designed and simulated using 180 nm CMOS technology on cadence spectre with supply voltage of 0.5V. The aspect ratio of transistors used to design this current mirror were 3/1 for M1 and M2, 2/2 for M3, M4 and M5. The W/L ratio of M6 is 10/0.3 with biasing current I_B of 1 μA and I_{B1} of 10 μA. The chosen values of C1 and C2 are 0.7pF and 0.3pF.

Fig. 6 shows the current transfer curve for input range of 0 to 200 μA with the error in current copying of 0.003% up to 100 μA as shown in the figure 7. The bandwidth of proposed current mirror is 100Mhz as depicted in figure 8 and table no. 1 shows the comparison of proposed with existing current mirrors. The supply voltage is quite reduced using FGMOS technique with power consumption of 62.6 μW making it suitable for ultra-low power applications.

Table 1. Comparison of proposed current mirror

Performance factor	**[7]**	**[9]**	**[15]**	**[16]**	**Proposed**
Supply Voltage (V)	**±1**	**-1**	**1.2**	**1.2**	**0.5**
Supply Range(μA)	**0 -500**	**0-500**	**0-200**	**0-200**	**0-200**
Power Consumption(μW)	**--**	**--**	**--**	**--**	**62.6**
Input impdedance(Ω)	**650**	**661**	**15**	**100**	**14**
Output Impdedance(GΩ)	**0.003**	**0.326**	**5**	**>0.2**	**4.5**
No. of transistors	**09**	**08**	**06**	**05**	**06**

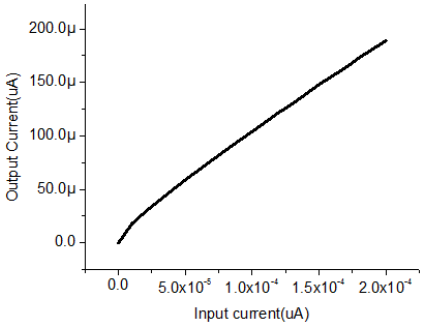


Figure 6: Current transfer curve

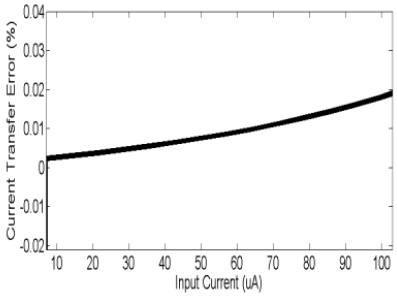


Figure 7: Error in current transfer

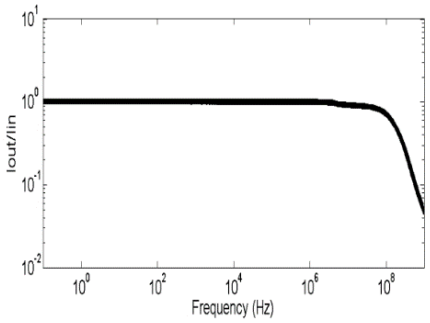


Figure 8: Frequency response of proposed current mirror

6 Conclusion

A low-voltage high performance FGMOS based current mirror has been proposed in this paper. The proposed implementation achieves the output impedance of 5GΩ and input impedance of 14Ω with increased input voltage swing at supply voltage of 0.5V. Current mirror is simulated using 180nm CMOS technology on cadence spectre to verify it. The design can be used in low power applications.

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