Contemporary Engineering Sciences, Vol. 10, 2017, no. 23, 1133 - 1142
HIKARI Ltd, www.m-hikari.com
https://doi.org/10.12988/ces.2017.79126

Circuit Design of 2-Input Reconfigurable Dynamic Logic Based on Stacked Type Fe-FET with Whole Set of 16 Functions

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Abstract

Circuit design of 2-input reconfigurable dynamic logic based on stacked type Fe-FET with the whole set of 16 functions has been newly described. This structure can be realized with low cost process technology of 3D NAND flash memory. By replacing +V for substrate to D-type Fe-FET and 0 for substrate to E-type Fe-FET logic generation part of newly proposed scheme can be realized with only 2 silicon pillars. This number of silicon pillars is only 1/3 compared with that of previously proposed conventional 16 function 12T DRDLC with two states (+V, 0) of control gate voltages scheme. By using process technology of 3D NAND flash memory low cost high density reconfigurable LSI will be realized with newly proposed scheme.

Keywords: reconfigurable logic, Fe-FET, stacked structure, logic LSI, 3D NAND

1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem various kinds of 3D transistors has been proposed. FinFET [2] [3] which

use the 3 planes as the channel for reducing the short channel effect has been developed. The application of FinFET which uses the same input for both sidewall channel to high end MPU begins. This is because the fabrication technology of FinFET is almost the same as that of the presently available conventional planar transistor except for the trench isolation for transistor formation.
On the other hand for reducing the number of transistors for logic circuit Independent-gate controlled Double Gate transistor, DG transistor, has been proposed [4]. Independent-gate controlled Double Gate transistor uses the sidewall as the channel with using two independent input signal. Therefore, two conventional planar transistors connected in series or parallel can be reduced to one Independent-gate controlled Double Gate transistor by controlling device parameters such as the impurity concentration of body or gate oxide thickness [5]. Various kinds of logic circuit is designed using this structure [6] [7]. Independent-gate controlled Double Gate transistor is promising candidate for the next generation of FinFET.
Furthermore, by using first gate for input signal and second gate for control signal Independent-gate controlled Double Gate transistor (DG MOS FET) can be used for the dynamic reconfigurable logic. First report for this application was 2-input dynamically reconfigurable dynamic logic circuit (DRDLC) with 5 transistors using three states (+V, 0, -V) of the control gate voltages [8]. Using this circuit 4 logic functions can be realized. However, this value of 4 is too small compared to 2^4=16 which is required for two Boolean input circuit.
In order to overcome this problem DRDLC which generate the whole set of 16 functions has been proposed [9]. In ref [9] 16 functions has been successfully realized by using 12 DCMOS FETs. The logic generation part except precharge, evaluation transistors and inverters of this circuit can be realized only 6 DGMOS FETs. This small number of 6 leads to small pattern area and the fabrication cost which is proportion to pattern area. 6 transistors are consists with 6 silicon pillar, because 1 layered structure is assumed. However, further smaller pattern area for this circuit part is required for realizing further low cost high density logic LSI. In this paper 16 functions 2-input reconfigurable dynamic logic based on stacked type Fe-FET has been newly proposed for satisfying this requirement.
This paper is organized as follows. In section 2 previously proposed conventional 16 functions 2-input reconfigurable dynamic logic based on DG MOS FET has been described. In section 3, a novel 16 functions 2-input reconfigurable dynamic logic based on stacked type Fe-FET has been described. In section 4, number of transisitors, silicon pillars and pattern area of logic generation part of this circuit are compared between proposed and conventional scheme. Finally, a conclusion of this work is provided in Section 5.

2 Previously proposed conventional 16 function 12 DRDLC using two states of control gate voltages(+V,0)

Previously proposed conventional 16 function 12T DRDLC is shown in Fig.1 [9].

This circuit consists with 12 transistors using two states (+V, 0), six configuration inputs (C1-C6), and two clock inputs (CLK, /CLK). Table 1 shows the configuration inputs and the corresponding inputs and corresponding logic function of $\overline{Y}$.

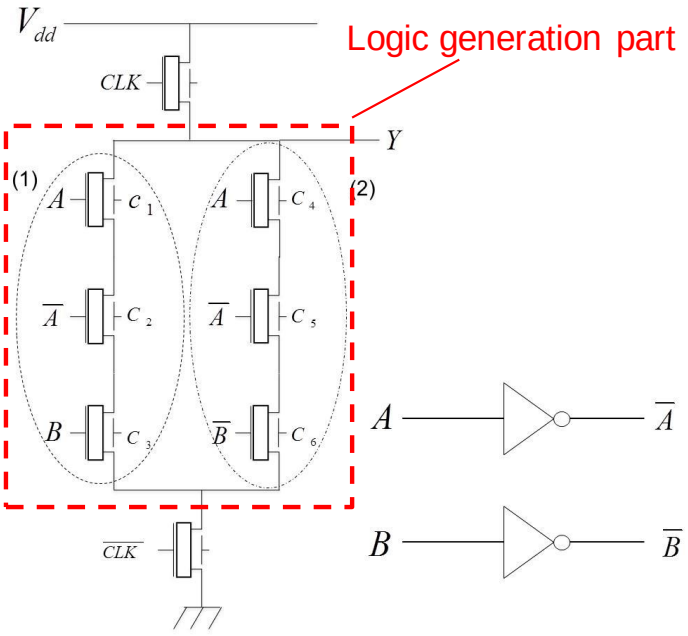


Figure 1: Previously proposed conventional 16-function 12T DRDLC with two states (+V, 0).

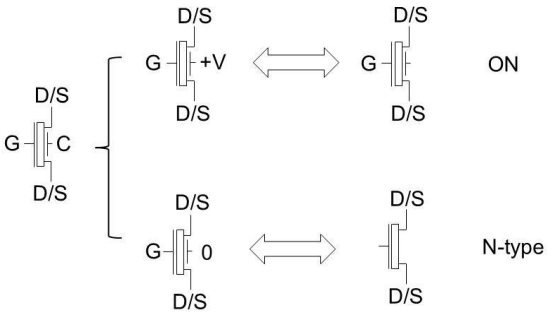


Figure 2: Previously proposed conventional DG-MOSFET device symbol and configurations with two state (+V, 0) used in Fig.1

Table 1: Configuration inputs and corresponding logic functions for previously proposed conventional 16-function 12T DRDLC with two state (+V, 0).

C_1	C_2	C_3	C_4	C_5	C_6	$\overline{Y}$
0	+V	0	0	0	+V	AB
+V	0	0	0	0	+V	$\overline{A}B$
0	0	+V	0	+V	0	$A\overline{B}$
0	0	+V	+V	0	0	$\overline{A}\overline{B}$
+V	0	0	0	+V	0	$A \oplus B$
0	+V	0	+V	0	0	$\overline{A \oplus B}$
0	+V	0	0	+V	0	A
+V	0	0	+V	0	0	$\overline{A}$
+V	+V	0	0	0	+V	B
0	0	+V	+V	+V	0	$\overline{B}$
+V	+V	0	0	+V	+V	$A + B$
+V	+V	0	+V	0	+V	$\overline{A} + B$
0	+V	+V	+V	+V	0	$A + \overline{B}$
+V	0	+V	+V	+V	0	$\overline{A} + \overline{B}$
+V	+V	+V	+V	+V	+V	T
0	0	+V	0	0	+V	$\perp$

For realizing two states of the control gate voltages, (+V, 0) scheme has been employed(Fig.2). The configuration input control DG-MOSFET as on-state for +V, N-type configuration for 0 as shown in Fig.2. By using this scheme 16 functions can be successfully realized with only 12 transistors. 6 transistors included in dashed line in Fig.1 is key logic generation part. This small number of 6 leads to small pattern area. This small number of 6 leads to small pattern area and the fabrication cost which is proportion to pattern area. However, further smaller pattern area for this circuit part is required for realizing further low cost high density logic LSI.

3 Newly proposed 16 functions 2-input reconfigurable dynamic logic based on stacked type Fe-FET

For further reduction of pattern area for previously proposed conventional scheme stacked type Fe-FET scheme with 3D NAND flash memory technology[10]-[15] has been newly proposed. For realizing newly proposed scheme which is the same operation as previously proposed conventional scheme Fe-FET device symbol as shown in Fig.3 is adopted. This scheme is the same structure as previously proposed conventional scheme which is shown in Fig.2. The +V configuration to

substrate for previous proposed scheme can be realized with D-type Fe-FET for newly proposed scheme. The 0 configuration to substrate for previous proposed scheme can be realized with E-type Fe-FET for newly proposed scheme. D-type Fe-FET is realized with previous program operation which is performed with application of high voltage between gate and substrate electrode of Fe-FET.

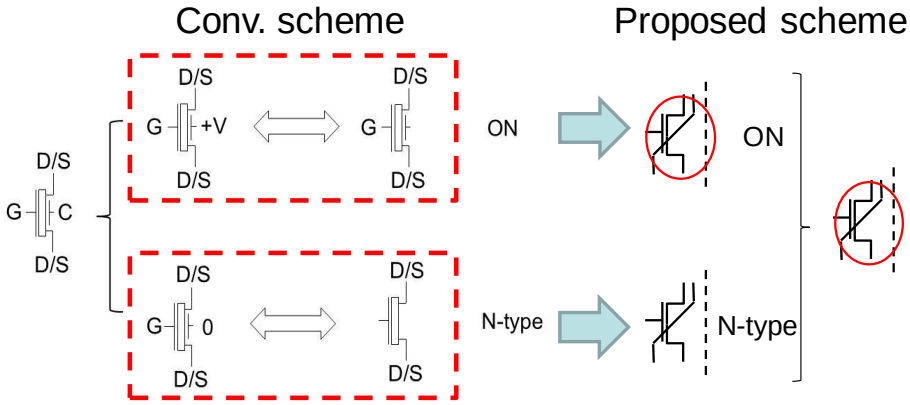


Figure 3: Newly proposed Fe-EFTs device symbol and configurations with two state (D-type, E-type) which is the same structure as previously proposed scheme.

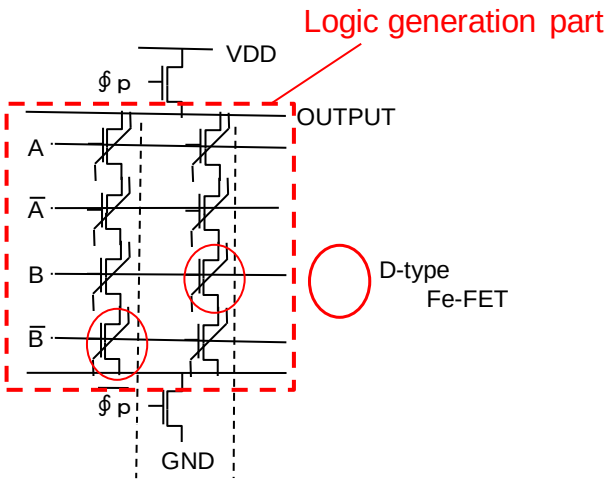
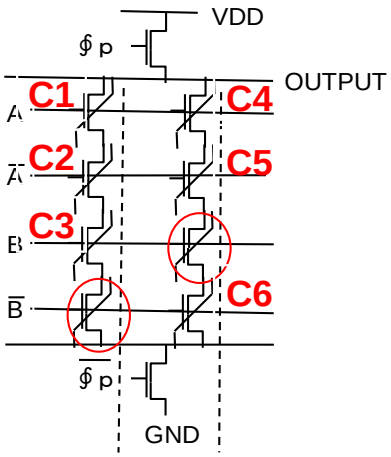


Figure 4: Newly proposed 16-function stacked Fe-FET scheme with two state (D-type, E-type).

The newly proposed logic correspond to Fig.1 except inverters is shown in Fig.4. Logic generation part with 6 transistors of Fig.1 is realized with 8 Fe-FET. 2 more D-type Fe-FET should be employed for realizing for pass transistor operation compared with Fig.1. This is because for stacked scheme all input signal must be inputted to Fe-FET which is connected in series. By using newly proposed scheme shown in Fig.4 16 functions can be successfully realized with only change +V of table1 to D-type Fe-FET as shown in table.3 and Fig.5.

Table 2: Configuration inputs and corresponding logic functions for newly proposed 16-function stacked Fe-FET scheme.

C_1	C_2	C_3	C_4	C_5	C_6	$\overline{Y}$
0	+V	0	0	0	+V	AB
+V	0	0	0	0	+V	$\overline{A}B$
0	0	+V	0	+V	0	$A\overline{B}$
0	0	+V	+V	0	0	$\overline{AB}$
+V	0	0	0	+V	0	$A \oplus B$
0	+V	0	+V	0	0	$\overline{A \oplus B}$
0	+V	0	0	+V	0	A
+V	0	0	+V	0	0	$\overline{A}$
+V	+V	0	0	0	+V	B
0	0	+V	+V	+V	0	$\overline{B}$
+V	+V	0	0	+V	+V	$A+B$
+V	+V	0	+V	0	+V	$\overline{A} + B$
0	+V	+V	+V	+V	0	$A + \overline{B}$
+V	0	+V	+V	+V	0	$\overline{A} + \overline{B}$
+V	+V	+V	+V	+V	+V	T
0	0	+V	0	0	+V	$\perp$



For example $A\overline{B}$ logic for $\overline{Y}$ can be realized with 2 D-type Fe-FET (C3,C5) as shown in left hand slide of Fig.5. B logic for $\overline{Y}$ can be realized with 3 D-type Fe-FET (C1,C2,C6) as shown in right hand slide of Fig.5.

4 Estimation of number of transistors, silicon pillars and pattern area

The number of transistors for logic generation part for newly proposed scheme of 8 is larger than that 6 of previously proposed conventional scheme. However, pattern area of newly proposed scheme can be smaller than that with conventional scheme. This is because the pattern area of newly proposed scheme with stacked structure is not in proportion to number of transistor but number of silicon pillar. Therefore, 8 Fe-FET for stacked structure can be realized with only 2 silicon pillars. For 1 layered case for conventional scheme the number of transistor of 6 is equal to the number of silicon pillars of 6. As a result, the pattern area of newly proposed scheme can be reduced to 2/6=1/3 compared with that for conventional case as shown in table 3. In table 3 not only newly proposed stacked structure but also another stacked structure (Fig.6) are also shown. Fig.6 scheme is useful for

realizing LUT for logic LSI and FPGA. Among 4 memory datum only one data can be selected through multiplexer circuit with is located on the memory devices. With another stacked structure 16 functions can be realized as the same as newly proposed scheme [16] [17]. The number of silicon pillar of 4 with another stacked structure can be successfully reduced to 1/2 of 2 with newly proposed stacked structure. From these estimation newly proposed scheme is promising candidate for realizing future low cost high density reconfigurable LSIs. Further research about fabrication cost [18] will be proposed near future.

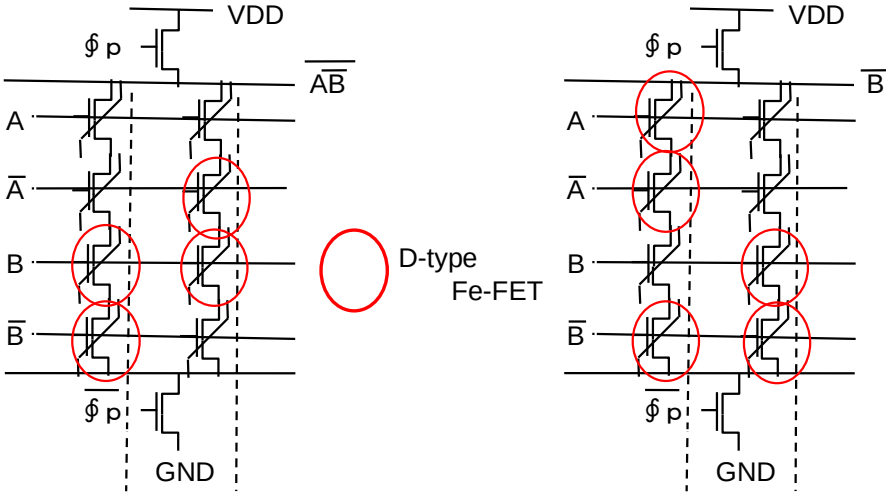


Figure 5: Formations of 2 logics with newly proposed stacked Fe-FET scheme.

Table 3: Comparison of number of transistor, silicon pillar and pattern area for logic generation part.

	Previous Conv. 1 layered type	**Newly proposed stacked type**	**another stacked type**
Number of Tr.	6	8	20
Number of Si Pillar	6	2	4
Normalized Pattern area	1	0.33	0.67

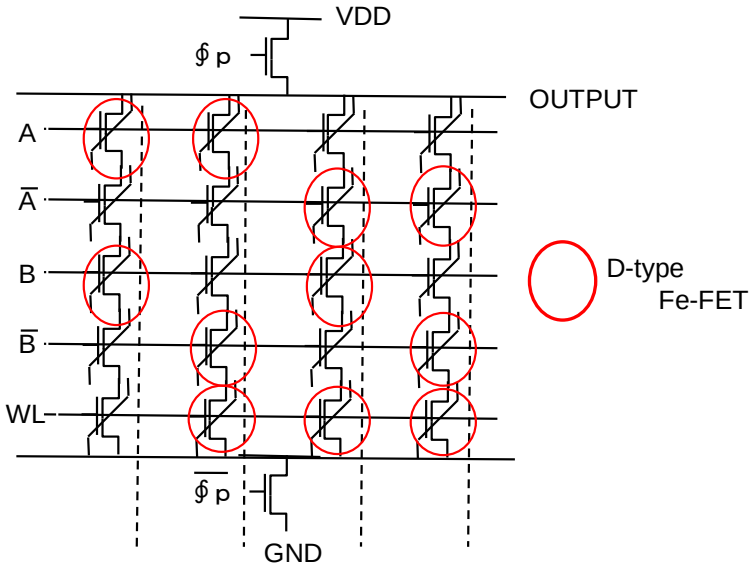


Figure 6: Another 16-function stacked Fe-FET scheme with two state (D-type, E-type).

5 Conclusion

Circuit design of 2-input reconfigurable dynamic logic based on stacked type Fe-FET with the whole set of 16 functions has been newly described. This structure can be realized with low cost process technology of 3D NAND flash memory. By replacing +V for substrate to D-type Fe-FET and 0 for substrate to E-type Fe-FET logic generation part of newly proposed scheme can be realized with only 2 silicon pillars. This number of silicon pillars is only 1/3 compared with that of previously proposed conventional 16 function 12T DRDLC with two states (+V, 0) of control gate voltages scheme. By using process technology of 3D NAND flash memory low cost high density reconfigurable LSI will be realized with newly proposed scheme.

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Received: October 16, 2017; Published: November 17, 2017