Contemporary Engineering Sciences, Vol. 10, 2017, no. 23, 1123 - 1132
HIKARI Ltd, www.m-hikari.com
https://doi.org/10.12988/ces.2017.79119

A Novel Horizontal Channel NAND Structure for Vertically Stacked Type System LSI

Tomohiro Yokota

DNP data techno Co., Ltd. Warabi-shi, Saitama, Japan

Shigeyoshi Watanabe

Department of Information Science
Shonan Institute of Technology, Fujisawa, Japan

Copyright © 2017 Tomohiro Yokota and Shigeyoshi Watanabe. This article is distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Abstract

In order to overcome the upper limit of number of stacked layer, a novel horizontal channel NAND structure for vertically stacked type system LSI has been newly proposed. The novel structure is featured with horizontal channel structure in which signal of NAND logic runs horizontal direction. By using newly proposed scheme low fabrication cost can be successfully realized without sacrificing high speed operation. For example, for the larger number of stacked layer case, such as 256 or 512 layer the delay time of newly proposed scheme with 32 Fe-FET connected in series can be reduced to 1/64 or 1/256 compared with that of previously proposed vertical channel case. Proposed scheme is promising candidates for realizing low cost and high speed vertically stacked system LSI.

Keywords: SGT, vertically stacked structure, horizontal channel, Fe-FET, system LSI, logic circuit

1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem FinFET [2] [3] which use the 3 planes and SGT (Surrounding Gate Transistor) [4] which use the 4 planes as the channel for reducing the short channel

effect has been developed. By using SGT not only reduction the short channel effect but also the reduction of the pattern area compared with that of the conventional planar transistor can be realized. This is because not only the planar region but also the sidewall can be used as the channel for this newly proposed structure.
The structure of SGT is shown in Fig.1. Four sidewalls can be used as the channel. Assuming that the sidewall channel width is defined as Ws, within the small pattern area large total channel width of 4Ws can be successfully realized. The drain current flows along vertical direction which is perpendicular to the conventional planar transistor case.

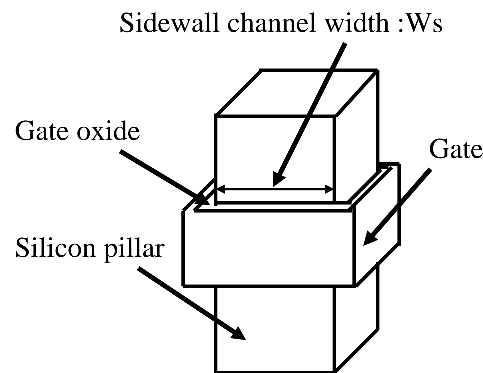

Figure 1: Structure of 1 layered SGT

Firstly, the research of LSI with 1 layered SGT is focused on the device technology of transistor and memory such as DRAM [5]-[9] and system LSI [10]-[11].

Recently, this SGT has been successfully applied to the vertically stacked type system LSI [12]-[13]. The applied vertically stacked type NAND/NAND array is shown in Fig.2. NAND logic is formed within the silicon pillar in which the signal runs to the vertical direction. Namely the vertical channel is employed. The output of NAND logic is formed on the silicon pillar. This structure is fabricated by using low cost process technology for 3D NAND flash memory [14]-[17]. For realizing low cost the number of stacked layer should be increased. However, the larger number of stacked layer results in the increase in the delay time of NAND logic.

In this paper, in order to overcome the upper limit of number of stacked layer, a novel horizontal channel NAND structure for vertically stacked type system LSI has been newly proposed. The novel structure is featured with horizontal channel structure in which signal of NAND logic runs horizontal direction. The novel structure can be realized by using another vertical stacked structure named vertical gate structure (horizontal channel structure) [18] [19].

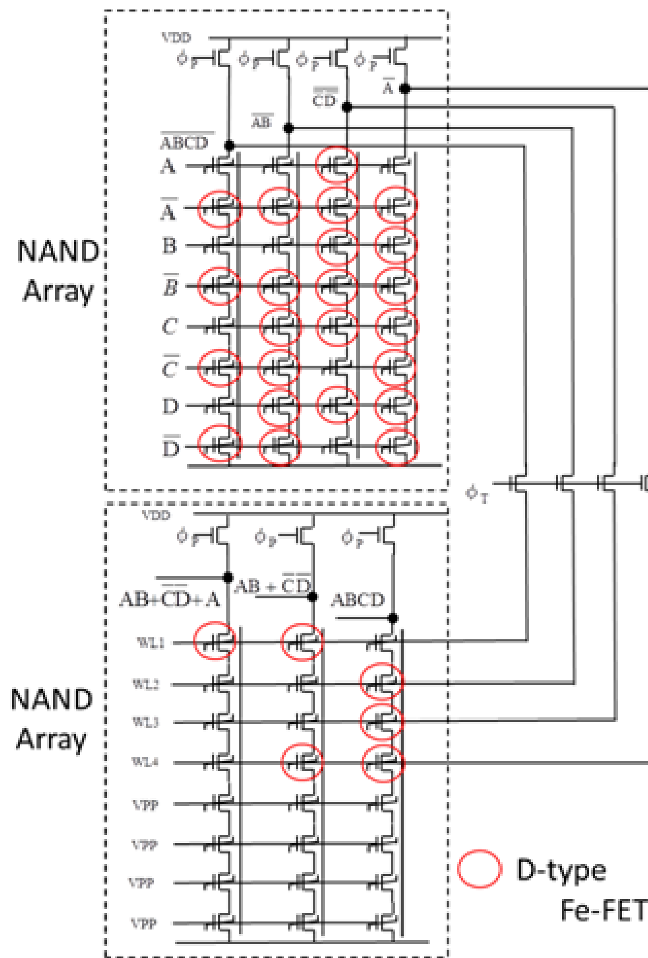

Figure 2: Vertically stacked type NAND/NAND array

2 Structure of horizontal channel NAND structure for vertically stacked type system LSI

The structure of proposed horizontal channel NAND structure is shown in Fig.3. The novel structure is featured with horizontal channel structure in which signal of NAND logic runs through horizontal direction. The channel is formed with Fe-FET and the input signal of NAND logic WL1-WL4 are inputted to the gates of Fe-FET. The output of NAND logic BL1-BL4 is outputted to right side edge of array structure. The operation scheme is the same as the previously proposed vertical channel scheme [12]-[13]. The size of Fe-FET for newly proposed scheme is 2F*2F=4F2, the same value of vertical channel case as shown in Fig.4. The width of Fe-FET, WL, and channel is F. The distance between adjacent channels and WLs is F, where F is design rule.

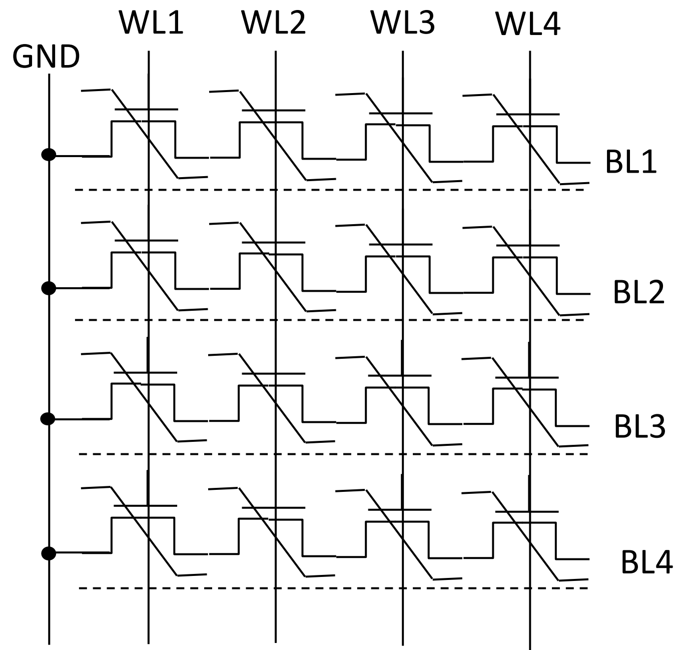

Figure 3: Structure of proposed horizontal channel NAND structure

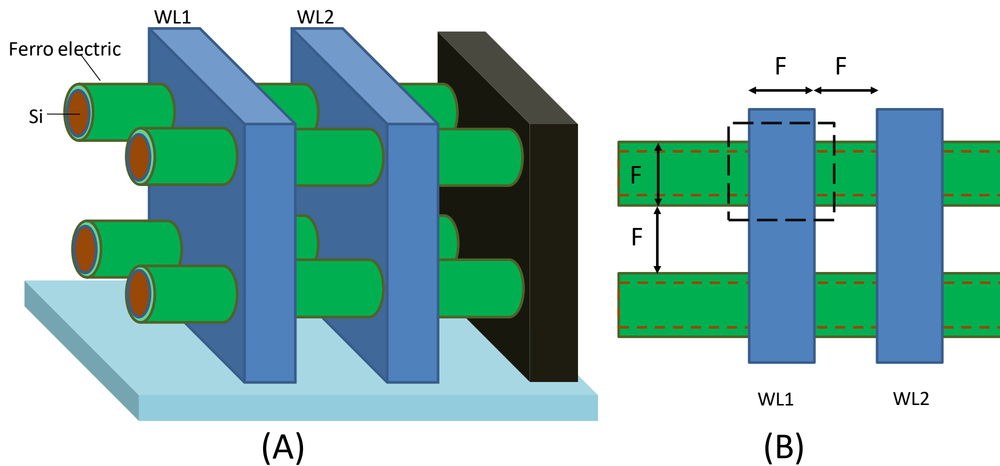

Figure 4: Structure of Fe-FET for proposed horizontal channel NAND structure (a)Top view, (b)Cross sectional view along channel direction

The process flow of proposed scheme is shown in Fig.5 and Fig.6. Firstly Si and SiGe are stacked vertically. This procedure is the same as that of vertical channel case. Next, to separates the adjacent Fe-FET Si and SiGe are selectively etched. Then, SiGe is removed for the formation of ferroelectric film and WL. Finally, ferroelectric film and WL are formed.

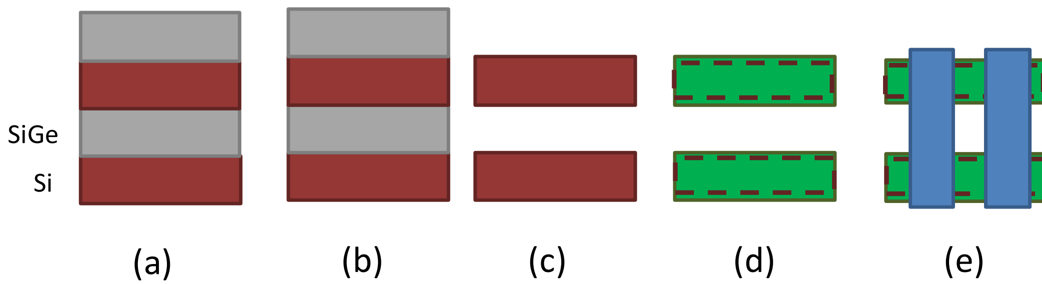

Figure 5: The process flow of proposed scheme for cross-sectional view along channel direction. (a)Formation of Si and SiGe, (b)Etching process of Si and SiGe, (c)Removal of SiGe, (d)Formation of ferroelectric film, (e) Formation of WL.

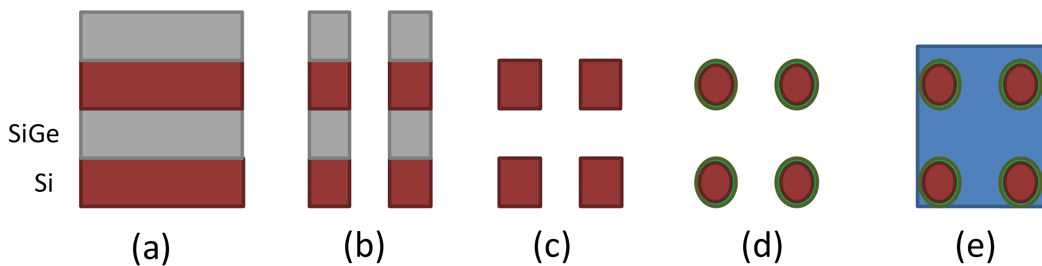

Figure 6: The process flow of proposed scheme for cross-sectional view perpendicular to channel direction. (a)Formation of Si and SiGe, (b)Etching process of Si and SiGe, (c)Removal of SiGe, (d)Formation of ferroelectric film, (e) Formation of WL.

For the newly proposed scheme number of Fe-FET connected in series and number of stacked layer can be determined independently. Therefore, both the low fabrication cost and high speed performance can be successfully realized. The delay time of NAND logic for both previously and newly proposed scheme are shown in Fig.7. The data for estimation of delay time is shown in Fig.8. F=39nm, and mobility of Fe-FET of 200cm2/Vs[20]-[24] are used. For the larger number of stacked layer case, such as 256 or 512 layer, the delay time of newly proposed scheme with 32 Fe-FET connected in series can be reduced to 1/64 or 1/256 compared with that of previously proposed case.

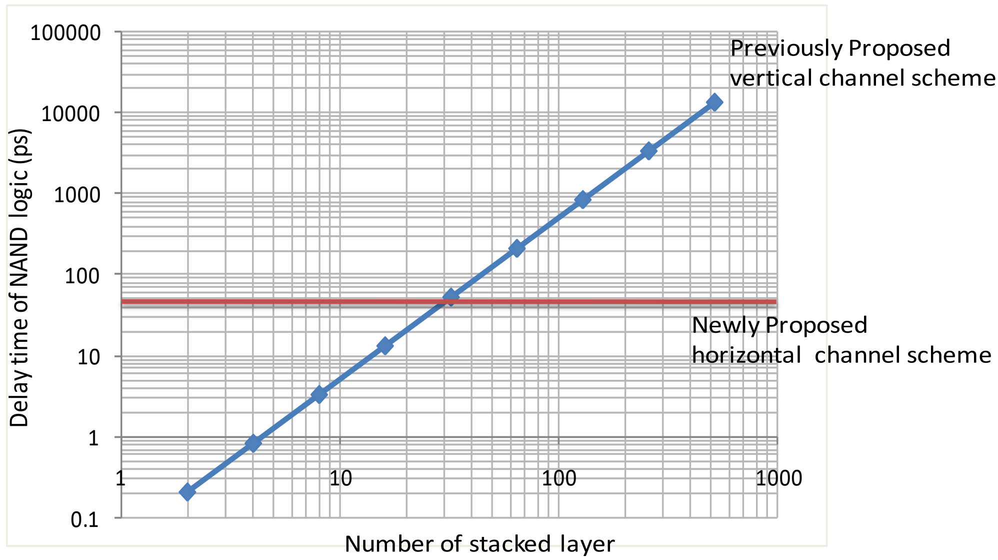

Figure 7: The delay time of NAND logic for both previously and newly proposed scheme.

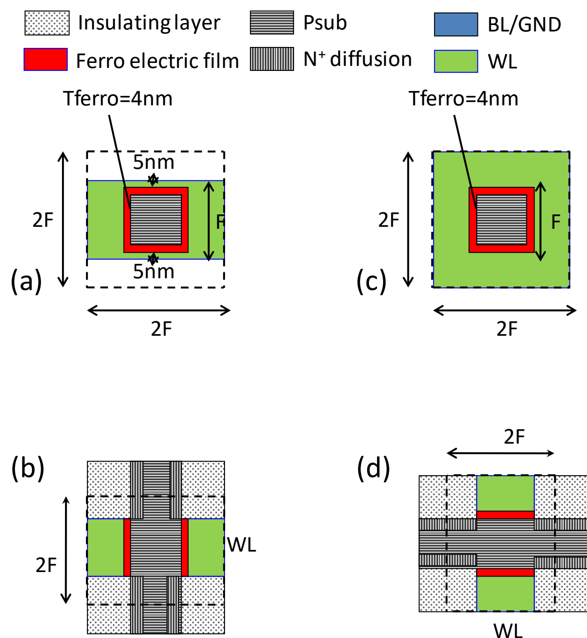

Figure 8: Cross-sectional view, (a)perpendicular to channel direction for previously proposed scheme, (b) along to channel direction for previously proposed scheme, (c)perpendicular to channel direction for newly proposed scheme, (d)along to channel direction for newly proposed scheme

3 Conclusion

In order to overcome the upper limit of number of stacked layer, a novel horizontal channel NAND structure for vertically stacked type system LSI has been newly proposed. The novel structure is featured with horizontal channel structure in which signal of NAND logic runs horizontal direction. By using newly proposed scheme low fabrication cost can be successfully realized without sacrificing high speed operation. For example, for the larger number of stacked layer case, such as 256 or 512 layer, the delay time of newly proposed scheme with 32 Fe-FET connected in series can be reduced to 1/64 or 1/256 compared with that of previously proposed vertical channel case. Proposed scheme is promising candidates for realizing low cost and high speed vertically stacked system LSI.

References

[1] International Technology Roadmap of Semiconductor 2003 Edition, 2003 Semiconductor Industry Association.

[2] K. Hieda, F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue, T. Hamamoto, Effect of a new trench-isolated transistor using side wall gates, *IEEE Trans. Electron Devices*, **36** (1989), no. 9, 1615-1619. https://doi.org/10.1109/16.34221

[3] Chenming Hu, J. Bokor, Tsu-Jae King, E. Anderson, C. Kuo, K. Asano, H. Takeuchi, J. Kedzierski, Wen-Chin Lee, D. Hisamoto, FinFET a self-aligned double gate MOSFET scarable to 20nm, *IEEE Trans. Electron Devices*, **47** (2000), no. 12, 2320-2325. https://doi.org/10.1109/16.887014

[4] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, F. Masuoka, Impact of surrounding gate transistor SGT for ultra-high-density LSIs, *IEEE Trans. Electron Devices*, **38** (1991), 573-578.
https://doi.org/10.1109/16.75168

[5] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi, F. Masuoka, Multi-pillar surrounding gate transistor (M-SGT) for compact and high-speed circuits, *IEEE Trans. Electron Devices*, **38** (1991), no. 3, 579-583. https://doi.org/10.1109/16.75169

[6] K. Sunouchi, H. Takato, N. Okabe, T. Yamada, T. Ozaki, S. Inoue, K. Hashimoto, K. Hieda, A. Nitayama, F. Horiguchi, F. Masuoka, A surrounding gate transistor (SGT) cell for 64/256Mbit DRAMs, *International Technical Digest on Electron Devices Meeting*, (1989) 23-26. https://doi.org/10.1109/iedm.1989.74220

[7] S. Watanabe, K. Tsuchida, D. Takashima, Y. Oowaki, A. Nitayama, K. Hieda,

H. Takato, K. Sunouchi, F. Horiguchi, K. Ohuchi, F. Masuoka, H. Hara, A novel circuit technology with surrounding gate transistors (SGTs) for ultra high density DRAMs, *IEEE J. Solid-State Circuits*, **30** (1995), no. 9, 960-971. https://doi.org/10.1109/4.406391

[8] S. Tamai and S. Watanabe, Design method of stacked type MRAM with NAND structured cell, *Contemporary Engineering Sciences*, **6** (2013), no. 2, 69-86. https://doi.org/10.12988/ces.2013.13007

[9] S. Tamai and S. Watanabe, Design method of stacked type thermally assisted MRAM with NAND structured cell, *Contemporary Engineering Sciences*, **6** (2013), no. 4, 143-161. https://doi.org/10.12988/ces.2013.13014

[10] T. Yokota and S. Watanabe, Study of reduction of pattern area for system LSI with SGT, *IEICE Trans. on Electronics*, **J92-C** (2009), no. 9, 537-539.

[11] T. Yokota and S. Watanabe, Analysis of pattern area reduction for logic circuit and system LSI with SGT, *Contemporary Engineering Sciences*, **8** (2015), no. 13, 589-601. https://doi.org/10.12988/ces.2015.54134

[12] T. Yokota and S. Watanabe, Proposal of vertical stacked type Fe－FET NAND/NAND array and its application to logic LSI, *IEICE. Trans. on Electronics*, **J99-C** (2016), no. 4, 150-159.

[13] T. Yokota and S. Watanabe, Proposal of vertical stacked type Fe-FET sequential logic circuit, *IEICE. Trans. on Electronics*, **J99-C** (2016), no. 7, 338-346.

[14] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, A. Nitayama, Bit Cost scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory, *2007 IEEE Symposium on VLSI Technology*, IEEE, 2007. https://doi.org/10.1109/vlsit.2007.4339708

[15] R. Katsumata, Masaru Kito, Yoshiaki Fukuzumi, Masaru Kido, Hiroyasu, Tanaka, Yosuke Komori, Megumi Ishiduki, Junya Matsunami, Tomoko Fujiwara, Yuzo Nagata, Li Zhang, Yoshihisa Iwata, Ryouhei Kirisawa, Hideaki Aochi, Akihiro Nitayama, Pipe-shaped BiCS flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices, *2009 Symp. on VLSI Technology*, IEEE, 2009, 136-137.

[16] J. Jang Han-Soo Kim, Wonseok Cho, Hoosung Cho, Jinho Kim, Sun Il Shim, Younggoan, Jae-Hun Jeong, Byoung-Keun Son, Dong Woo Kim, Kihyun, Jae-Joo Shim, Jin Soo Lim, Kyoung-Hoon Kim, Su Youn Yi, Ju-Young Lim, Dewill Chung, Hui-Chang Moon, Sungmin Hwang, Jong-Wook Lee, Yong-Hoon Son,

U-In Chung, Won-Seong Lee, Vertical cell array using TCAT(Terabit Cell Array Transistor) technology for ultra high density NAND flash memory, *2009 Symp. on VLSI Technology*, IEEE, 2009, 192-193.

[17] J-W. Im, W-P. Jeong, D-H. Kim, S-W. Nam, D-K. Shim, M-H. Choi, H-J. Yoon, D-H. Kim, Y-S. Kim, H-W. Park, D-H. Kwak, S-W. Park, S-M. Yoon, W-G. Hahn, J-H. Ryu, S-W. Shim, K-T. Kang, S-H. Choi, J-D. Ihm, Y-S. Min, I-M. Kim, D-S. Lee, J-H. Cho, O-S. Kwon, J-S. Lee, M-S. Kim, S-H. Joo, J-H. Jang, S-W. Hwang, D-S. Byeon, H-J. Yang, K-T. Park, K-H. Kyung, J-H. Choi, 7.2 A 128Gb 3b/cell V-NAND Flash Memory with 1Gb/s I/O Rate2, *2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers*, (2015). https://doi.org/10.1109/isscc.2015.7062960

[18] W. Kim, S. Choi, J. Sung, T. Lee, C. Park, H. Ko, J. Jung, I. Yoo, Y. Park, Multi-layered vertical gate NAND flash overcoming stacking limit for terabit density storage, *2009 Symposium on VLSI Technology*, IEEE, 2009.

[19] Jang-Gn Yun, G. Kim, Joung-Eob Lee, Y. Kim, W. Bo Shim, Jong-Ho Lee, H. Shin, J. D. Lee, Byung-Gook Park, Single-crystalline Si Stacked Array (STAR) NAND flash memory, *IEEE Transactions on Electron Devices*, **58** (2011), no. 4, 1006-1014. https://doi.org/10.1109/ted.2011.2107557

[20] E. Yurchuk, J. Muller, J. Paul, T. Schlosser, D. Martin, R. Hoffmann, S. Mueller, S. Slesazeck, U. Schroeder, R. Boschke, R. van Bentum, T. Mikolajick, Impact of Scaling on the Perfomance of HfO2 Based Ferroelectric Field Effect Transistors, *IEEE Trans. Electron Devices*, **61** (2014), 3699-3706. https://doi.org/10.1109/ted.2014.2354833

[21] T.P.-C. Juan, C. Chang, J.Y. Lee, A new metal - ferroelectric (PbZr0.57Ti0.43O3) – insulator (Dy2O3) semiconductor (MSIF) FET for nonvolatile memory applications, *IEEE Trans. Electron Device Lett.*, **27** (2006), no. 4, 217-220. https://doi.org/10.1109/led.2006.870414

[22] P. Sharma K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark, S. Datta, Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with Ferroelectric Hafunimm Zirconium oxide gate stack, *Symp. on VLSI Technology, Dig. Tech. Papers*, IEEE, 2017, T154-T155. https://doi.org/10.23919/vlsit.2017.7998160

[23] T. Nishimura, T. Yajima, K. Nagashio, A. Toriumi, Toward 1-nm-EOT Hf0.5Zr0.5o2 Ferroelectric films, *Extended Abstract of the 2014 International Conference on Solid State Devices and Materials*, (2014), 30-31. https://doi.org/10.7567/ssdm.2014.ps-1-13l

[24] K. Florent, S. Lavizzari, L. Di Piazza, M. Popovici, E. Vecchio, G. Potoms, G. Groeseneken, J. Van IHoudt, First demonstration of vertically stacked Ferroelectric AL Doped HfO2 decices for NAND applications, *Symp. on VLSI Technology, Dig. Tech. Papers*, IEEE, 2017, T158-T159.
https://doi.org/10.23919/vlsit.2017.7998162

Received: October 11, 2017; Published: November 17, 2017