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Low Cost Stacked Type NOR MRAM with 1 MOSFET/1 MTJ Cell Structure and Shared Source Line (SL) Scheme

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Abstract

In this paper stacked type NOR MRAM with 1 MOSFET/1 MTJ cell structure has been newly proposed. For realizing this structure new process steps for formation of MTJ has been introduced. Furthermore, for reducing bit cost novel shared source line (SL) scheme with VDD/2 precharge during write operation has been described. Estimated bit cost for stacked type NOR MRAM is very small, 0.03-0.31, compared with that of 1 layered NAND flash memory. This shows that not only NAND structure but also proposed scheme is promising candidate for realizing ultra low bit cost non-volatile memory. For the further reduction of bit cost the reduction of memory cell area is key issue.

Keywords: MRAM, NAND/NOR structured cell, spin transistor, MTJ, BiCS, bit cost

1 Introduction

DRAM is widely used for the main memory of personal computer because of its high speed characteristics. On the other hands, NAND flash memory which has the features of non-volatility and low bit cost is widely used for the storage device

of the multi-media data. Universal memory which has both features, DRAM and NAND flash memory, is key technology for the future memory system.
Recently, two types of stacked type MRAM have been proposed for the candidate of the universal memory [1]-[4]. First type is NAND structured architecture [1]-[3]. The bit line runs along the Z- direction and WL runs horizontal direction. This NAND structured architecture was already applied to Gbit stacked type flash memory [5]. 32 layer is applied for realizing Gbit density. This NAND structured architecture can be applied to ultra low cost stacked type MRAM which features 512-1024 stacked layer [6]-[8]. By using 512-1024 layer ultra low bit cost sufficient to replace presently available HDD can be realized.
Second type is NOR structured architecture [4]. The view of stacked type NOR MRAM memory cell array using BiCS structure [9] is shown in Fig.1 [4]. The bit line runs along horizontal direction and WL runs the Z- direction. By using this structure the fast access time competitive DRAM can be realized.

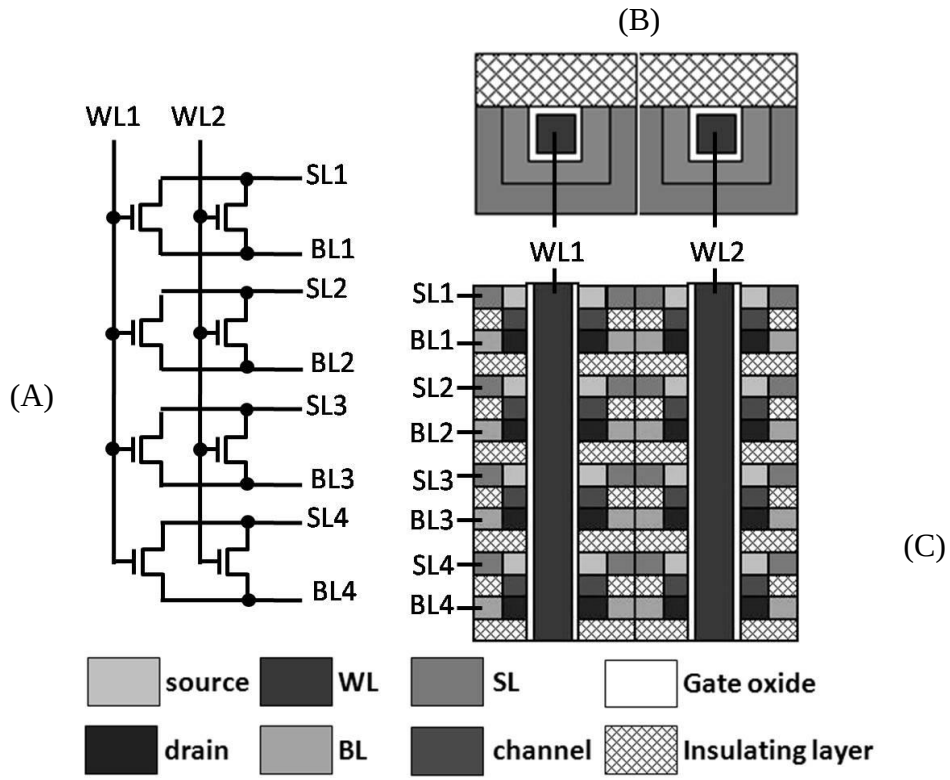

Figure 1: View of stacked type NOR MRAM memory cell array using spin transistor and BiCS structure, (A)circuit diagram, (B)top view, (C)cross-sectional view.

For the memory element for stacked type NOR MRAM spin transistor is adopted [10]. The source line (SL) is used for fixed layer and bit line is used for free layer for memory storage (Fig.2 (A)). Both switching function and storage function can be successfully realized by using 1 spin transistor. However, the spin transistor is now under research level. On the other hand conventional 1 MOSFET /1 MTJ

type MRAM is limited to 2-dimentional as the same as conventional system LSI. Stacked type MRAM with conventional 1 MOSFET /1 MTJ type cell structure has not been reported.

In this paper stacked type NOR MRAM with 1 MOSFET /1 MTJ type cell structure has been newly described. This paper is organized as follows. Section 2 describes the concept of stacked type NOR MRAM with 1 MOSFET /1 MTJ type cell structure. Section 3 presents the newly proposed shared Source Line (SL) scheme for realizing low bit cost. Finally, a conclusion of this work is provided in Section 4.

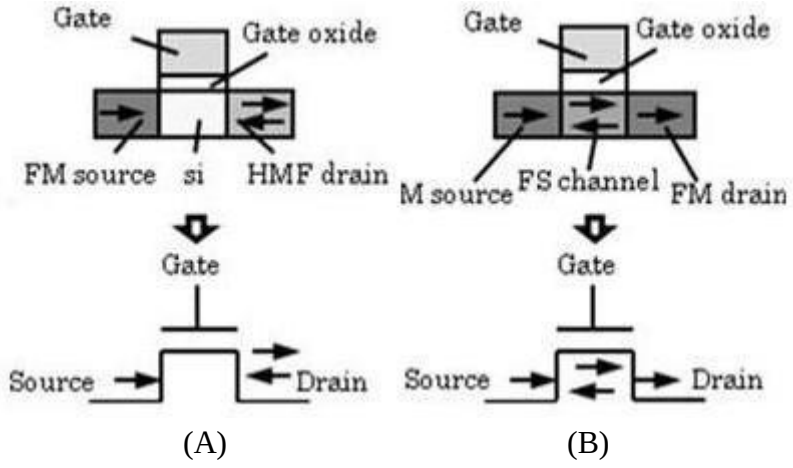

Figure: 2 Spin transistor and Equivalent circuit, (A)spin transistor for NOR MRAM, (B) spin transistor for NAND MRAM.

2 Concept of stacked type NOR MRAM with 1 MOSFET /1 MTJ type cell structure

The concept of newly proposed stacked type NOR MRAM with 1 MOSFET /1 MTJ type cell structure is shown in Fig.3. Conventional 1 MOSFET /1 MTJ type cell is stacked to Z direction. WL runs along Z direction and BLs and SLs run along horizontal direction. Adjacent SL, SL1 and SL2, is shared within adjacent cells for Z direction. Namely, SL1 and SL2 is merged as SL12 (SL3 and SL4 is merged as SL34). This shared source line architecture is newly proposed for reducing the number of process steps. This leads to the reduction of bit cost. Further discussion is described in section 3.

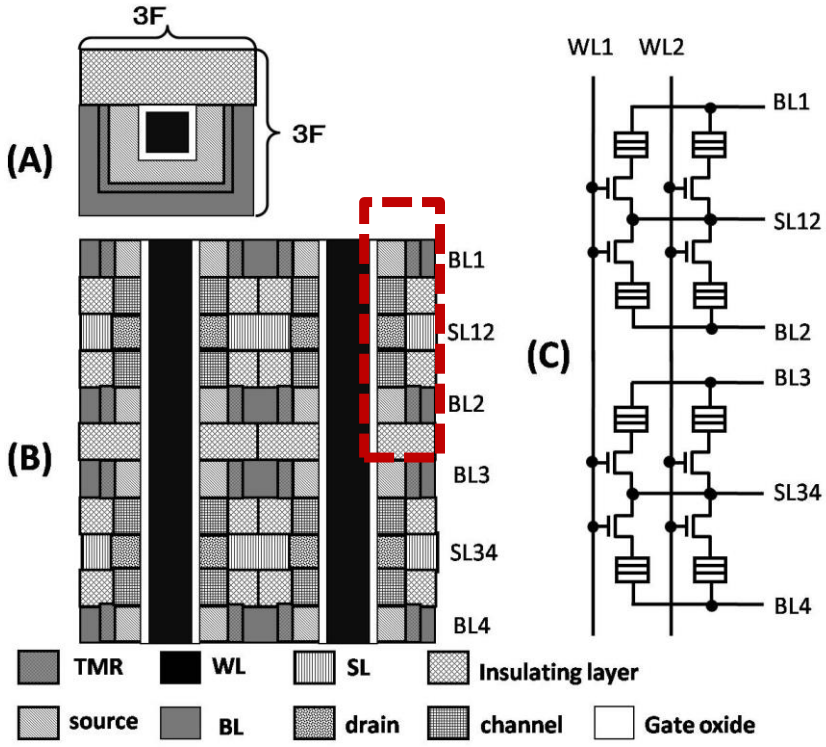

Figure 3: View of stacked type NOR MRAM memory cell array using 1 MOSFET /1 MTJ and BiCS structure, (A)top view, (B)cross-sectional view, (C)circuit diagram,.

The BL and shared SL is connected to drain and source electrode of MOSFET using sidewall. BL is formed with metal which contains N+ impurity. Shared SL is formed with metal featured by fixed layer characteristics. Furthermore, shared SL must contain N+ impurity, free layer material and dielectric layer material which is finally becomes the dielectric layer between free and fixed layer. This MOSFET is vertical SGT [11]-[13] type structure which uses three sidewalls as the channel. By using these structure stacked type NOR MRAM with 1 MOSFET /1 MTJ and BiCS structure can be successfully realized. The memory cell size is $3F*3F=9F^2$ which is the same value as previously proposed stacked type NOR MRAM [4].
The key technology for realizing newly proposed scheme is process technology for realizing sidewall diffusion of N+ for source and drain electrode, of free layer for drain electrode, and of dielectric layer between free and fixed layer. Process flow of proposed stacked cell within dashed line in Fig.3 (B) is shown in Fig.4. As shown in Fig.4 (A) these materials are already contained in stacked BLs (BL1 and BL2) and SL12. Namely, N+ impurity is contained in SL12 metal, and impurity for N+, dielectric, and free layer are contained in fixed layer of BLs. During 1st thermal treatment N+ is diffused within silicon from SL12 and BLs as shown in Fig.4 (B). These N+ form the source and drain electrode. Then, during

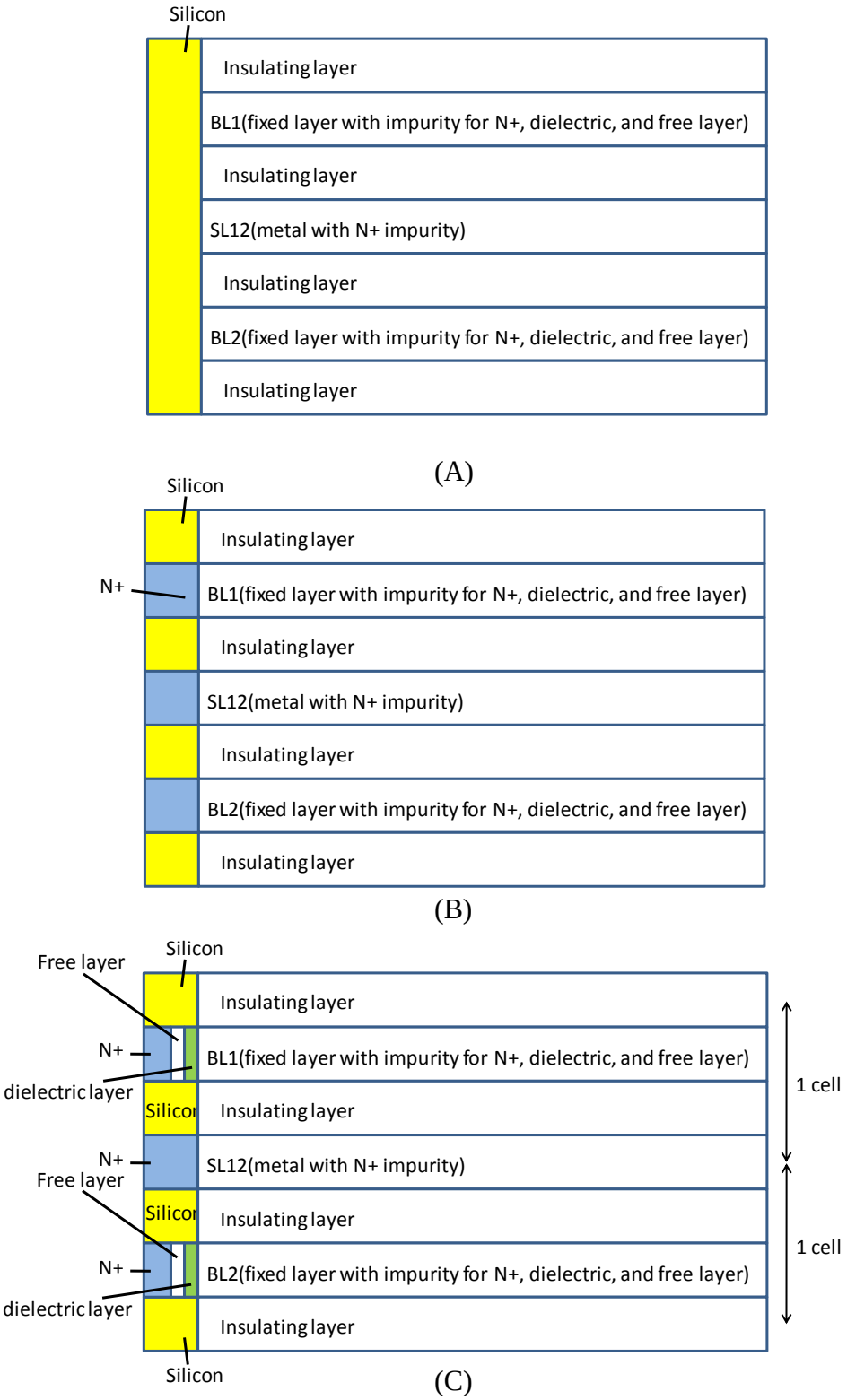

Figure 4: Process flow, (A)before thermal treatment, (B)after 1st thermal treatment, (C)after 2nd thermal treatment.

2nd thermal treatment free layer and dielectric layer are diffused from BLs as shown in Fig.4(C). Both free layer and dielectric layer are formed using the difference of diffusion constant between free layer and dielectric layer in the temperature of 2nd thermal treatment at the same time. Larger diffusion constant compared with that of dielectric layer is employed for free layer. This free layer, dielectric layer and fixed layer of BLs form the MTJ (Magnetic Tunneling Junction) for memory storage.

3 Shared Source Line (SL) scheme

For realizing low bit cost reduction of number of layer for realizing 1 stage of memory cell is critical issue. If for realizing 1 stage of memory SL is separated from next stage of memory cell as shown in Fig.5 (A), 4 layer (BL, insulating layer, SL, and insulator) must be adopted. This results in the increase in bit cost.
In order to overcome this problem shared source line (SL) scheme has been newly introduced as shown in Fig.5 (B). SL is shared with two stages of memory cells. That is, SL12 is shared SL. By using this scheme 1 stage of memory cell can be realized by using 3 layer (BL, insulating layer, SL/2, and insulator/2). This leads to the 3/4 bit cost compared with conventional separated SL scheme.

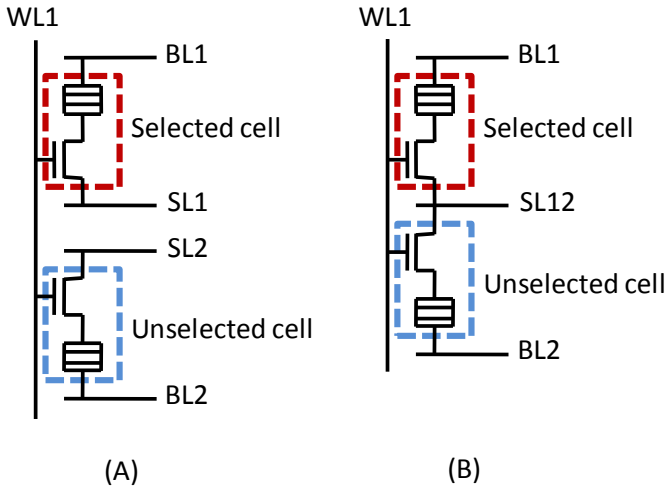

Figure 5: Configuration of memory cell array, (A)Conventional separated SL scheme, (B)Newly proposed shared SL scheme.

For realizing the shared SL scheme the precharge level of BL and SL is key issue for preventing miss writing to the unselected cell during write operation of selected cell (Fig.5). For the conventional separated SL scheme case miss writing does not occurred within the unselected cell independent to the precharge level before write operation. This is because SL2 and BL2 remain to the same prechage level during write operation of selected cell. The case of VDD prechage scheme is shown in Fig.6 (A). On the other hand in the newly proposed shared SL scheme case miss writing to the unselected cell occurs VDD or VSS precharge scheme.

The case of VDD precharge scheme is shown in Fig.6 (B). During write operation of selected cell SL12 and BL2 of unselected cell is equalized via the MOSFET and MTJ connected in series. However, because of resistance of MTJ (order of 1-10k ohm) the discharge of BL2 is delayed compared with that of SL12. This generates the large voltage difference between BL2 and SL12. This value is as large as VDD in the worst case. If the memory cell is written with large voltage difference of VDD between BL and SL, this leads to the miss wiring of unselected cell. This problem occurs in the VSS precharge case, too. In order to overcome this problem VDD/2 precharge scheme is key issue for the shared SL scheme. In this case voltage difference between BL2 and SL12 is limited to less than VDD/2 as shown in Fig.6 (C). This value is small enough for avoiding miss writing of unselected cell.

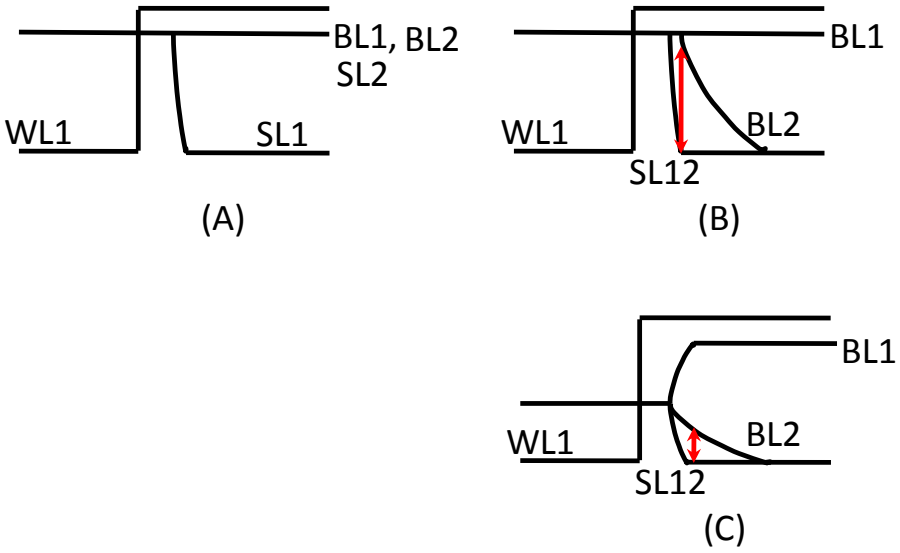

Figure 6: Miss operation of unselected cell, (A)conventional separated SL scheme of VDD precharge, (B) Shared SL scheme of VDD precharge, (C)Shared SL scheme of VDD/2 precharge.

These analysis is shown in the MTJ operation curve as shown in Fig.7. If 39nm design rule is adopted, the junction size of MTJ becomes F*5F=39nm*195nm. Fig.7 shows the measured characteristics which corresponds to almost the same junction size [14]-[16]. For the VDD prechage case current reach to the miss writing level. On the other hand the current is limited to the small value for VDD/2 precharge case. There is large current margin as shown in Fig.7.

Bit cost of memory cell array for stacked type NOR MRAM is estimated. The estimated procedure is the same as that of stacked type NAND MRAM case [6] [17]. Estimated bit cost of memory cell array for stacked type NOR/NAND

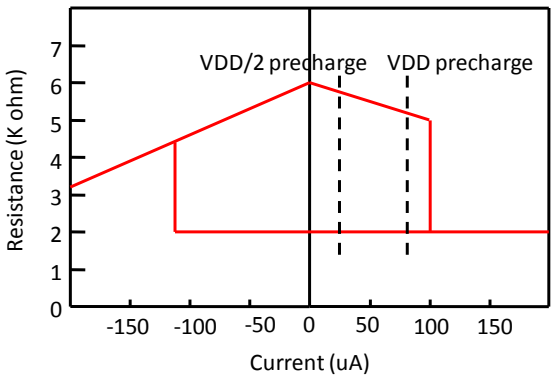

Figure 7: MTJ operation curve and generated current of unselected memory cell during write operation of selected cell for shared SL scheme.

MRAM vs number of layer is shown in Fig.8. The yield of 1 layer NAND flash memory, Y=95%, is used as a parameter. Two process cases, process steps/layer of 0.04 for conventional process and 0.004 for ultra low process [6], are considered. The memory cell size are the same value of $9F^2$. As for NOR MRAM both separated SL and shared SL scheme has been estimated. There is an optimized bit cost for all cases. For all cases the optimized bit cost is very small compared with that with 1 layered NAND flash memory. This shows that not only NAND structure but also NOR structure is promising candidate for realizing ultra low bit cost non-volatile memory. Especially bit cost of newly proposed shared SL scheme can be successfully reduce to 3/4 of that for conventional separated SL scheme. This shows that shared SL scheme is promising candidate for realizing ultra low bit cost non-volatile memory. For the further reduction of bit cost for NOR structure reduction of memory cell area are key issues.

	NAND		NOR			
			separated SL		shared SL	
process steps/layer	0.04	0.004	0.08	0.008	0.06	0.006
bit cost	0.2025	0.0206	0.4049	0.0412	0.3117	0.0305
optimized layer	64	512	32	256	32	512

Figure 8: Bit cost for cell array of stacked type NOR/NAND MRAM.

4 Conclusion

In this paper stacked type NOR MRAM with 1 MOSFET/1 MTJ cell structure has been newly proposed. For realizing this structure new process steps for formation of MTJ has been introduced. Furthermore, for reducing bit cost novel shared source line (SL) scheme with VDD/2 precharge during write operation has been described. Estimated bit cost for stacked type NOR MRAM is very small, 0.03-0.31, compared with that of 1 layered NAND flash memory. This shows that

not only NAND structure but also proposed scheme is promising candidate for realizing ultra low bit cost non-volatile memory. For the further reduction of bit cost the reduction of memory cell area is key issue.

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