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Process Step and Analysis of Bit Cost for Stacked Type MRAM with NOR Structured Cell

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Abstract

In this paper the process step and analysis of bit cost of stacked type MRAM with NOR structured cell has been newly described. For NOR structure 4 layer process is needed for realizing 1 layer memory cell compared with 2 layer for NAND structure. Estimated bit cost for stacked type NOR MRAM is very small, 0.04-0.4, compared with that of 1 layered NAND flash memory. This shows that not only NAND structure but also NOR structure is promising candidate for realizing ultra low bit cost non-volatile memory. For the further reduction of bit cost for NOR structure the reduction of process steps/layer and reduction of memory cell area are key issues.

Keywords: MRAM, NAND/NOR structured cell, spin transistor, BiCS, bit cost

1 Introduction

DRAM is widely used for the main memory of personal computer because of its high speed characteristics. On the other hands, NAND flash memory which has the features of non-volatility and low bit cost is widely used for the storage device of the multi-media data. Universal memory which has both features, DRAM and NAND flash memory, is key technology for the future memory system.
Recently, two types of stacked type MRAM have been proposed for the candidate of the universal memory [1]-[4]. First type is NAND structured architecture [1]-

[3]. The bit line runs along the Z- direction and WL runs horizontal direction. This NAND structured architecture was already applied to Gbit stacked type flash memory [5]. 32 layer is applied for realizing Gbit density. This NAND structured architecture can be applied to ultra low cost stacked type MRAM which features 512-1024 stacked layer [6]-[8]. The process step and bit cost has been presented and estimated in the previous paper [6] [9]. By using 512-1024 layer ultra low bit cost sufficient to replace presently available HDD can be realized.
Second type is NOR structured architecture (Fig.1) [4]. The view of stacked type NOR MRAM memory cell array using BiCS structure [10] is shown in Fig.1 [4]. The bit line runs along horizontal direction and WL runs the Z- direction. By using this structure the fast access time competitive DRAM can be realized. However, the process step and bit cost has not been reported.

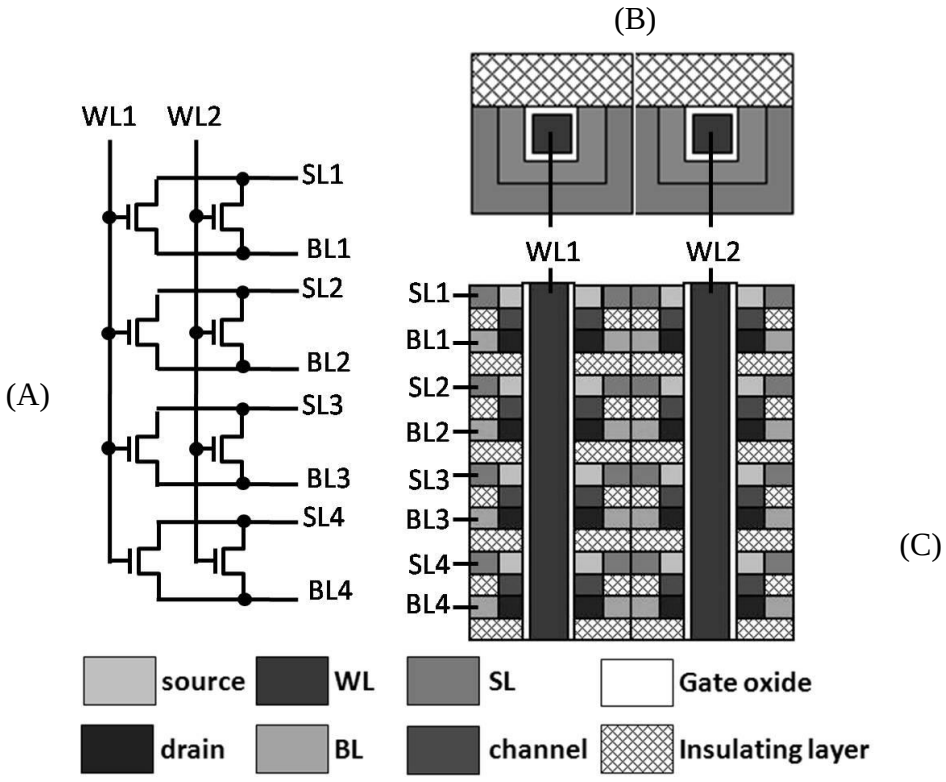

Figure 1: View of stacked type NOR MRAM memory cell array using BiCS structure, (A)circuit diagram, (B)top view, (C)cross-sectional view.

In this paper the process step and analysis of bit cost of stacked type MRAM with NOR structured cell has been newly described. This paper is organized as follows. Section 2 describes the process step of stacked type NOR MRAM. Section 3 presents the analysis of bit cost of memory cell array for stacked type NOR MRAM compared with previously reported stacked type NAND MRAM. Finally, a conclusion of this work is provided in Section 4.

2 Process step for stacked NOR MRAM

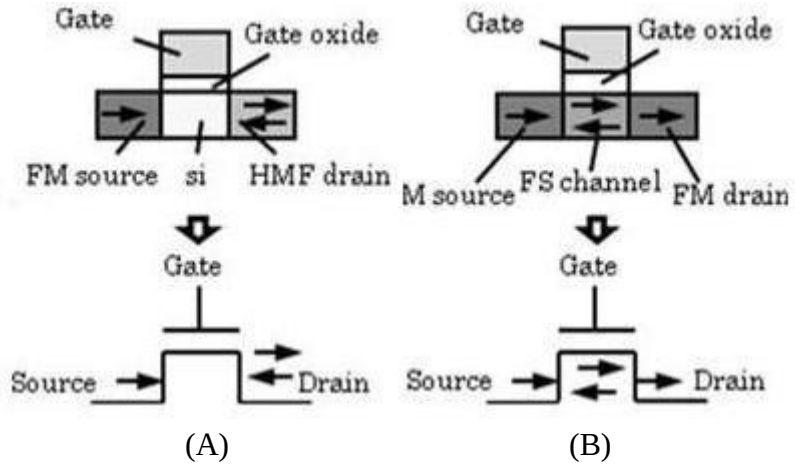

Figure:2 Spin transistor and Equivalent circuit, (A)spin transistor for NOR MRAM, (B) spin transistor for NAND MRAM.

For the memory element for stacked type NOR MRAM spin transistor is adopted [11]. The source line (SL) is used for fixed layer and bit line is used for free layer for memory storage (Fig.2 (A)). Two WLs and four BLs are shown for simplicity. The bit line runs along horizontal direction and WL runs the Z- direction. SLs and BLs are connected to source and drain electrode using sidewalls. The memory cell size is 3F*3F which is the same as that of stacked type NAND MRAM [1] [2]. The writing operation can be realized using spin torque operation which features low power consumption compared with magnetic writing scheme used for stacked type NAND MRAM [1] [2].

The process steps for stacked NOR MRAM is firstly described in Fig.3. First process step of formation of silicon pillar is shown in Fig.3 (A). This silicon pillar is finally used as source, channel and drain region of spin transistor. This silicon pillar is formed with high aspect ratio silicon etching process already used for stacked type NAND flash memory[5][10]. Trench aspect ratio of 100 is used for commercial base. After that 4 layers (isolation layer for free layer, layer for BL, isolation layer for fixed layer, and layer for SL) is formed for 1 layer memory cell, (Fig.3 (B)). These 4 layer process is needed for realizing 1 layer memory cell for stacked type NOR MRAM. In the stacked type NAND MRAM case this value, 4, can be reduced to 2, (isolation layer and layer for WL). As a result, bit cost of NOR MRAM case becomes larger than that of NAND MRAM case. In Fig.3 (D) 4 layer memory cell is assumed. As a result 4*4=16 layers are formed as shown in Fig.3 (D). After that for realizing gate oxide and WL trench within silicon pillar is

formed (Fig.3 (E)). After that gate oxide is formed within the trench (Fig.3 (F)). Next, thermal treatment is performed for forming fixed layer and free layer. These are realized diffusion process of fixed and free layer magnetic material from isolation layer. For realizing this process isolation layer for free layer must contain the magnetic material for free layer. And also, isolation layer for fixed layer must contain the magnetic material for fixed layer. This thermal treatment is key process for realizing both stacked type NOR and NAND MRAM. After that WL is formed within the trench (Fig.3 (H)). After that for the separation of adjacent memory cell trench formation (Fig.3 (I)) and isolation formation (Fig.3 (J)) are performed. The process steps of 7 for realizing NOR structure (silicon pillar, trench within memory cell, formation of gate oxide, formation of fixed/free layer, formation of WL, trench between adjacent memory cell, and formation of isolation) is almost the same as that for NAND MRAM case.

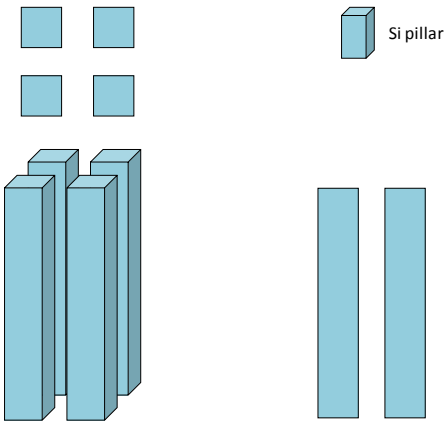

Figure 3 (A): Silicon pillar formation

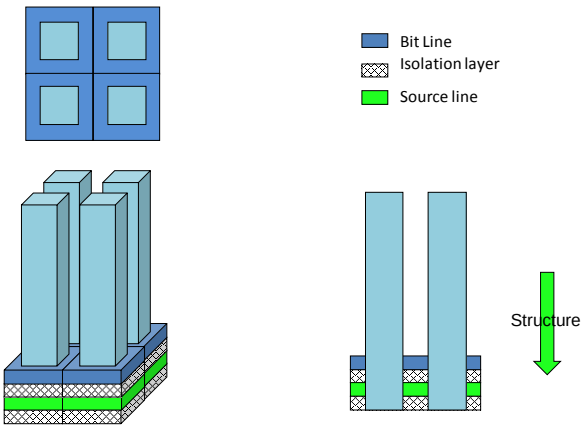

Figure 3 (B): Formation of 1st layer memory cell

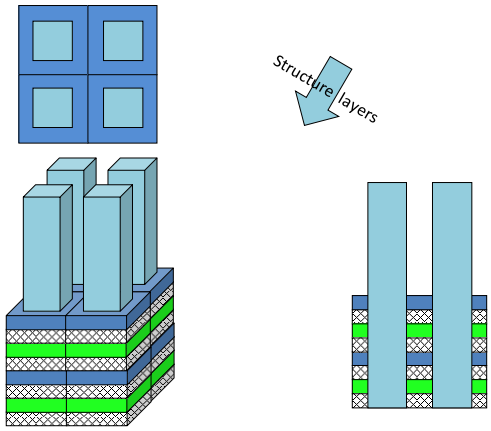

Figure 3 (C): Formation of 2nd layer memory cell

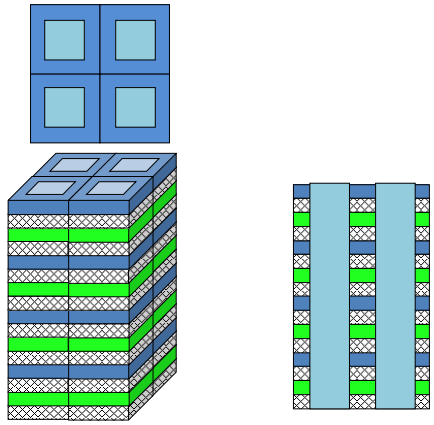

Figure 3 (D): Formation of final layer memory cell

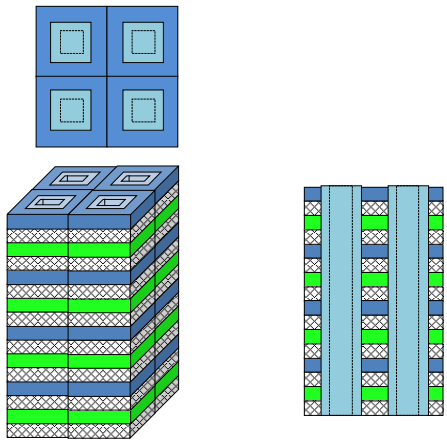

Figure 3 (E): Formation of trench within memory cell

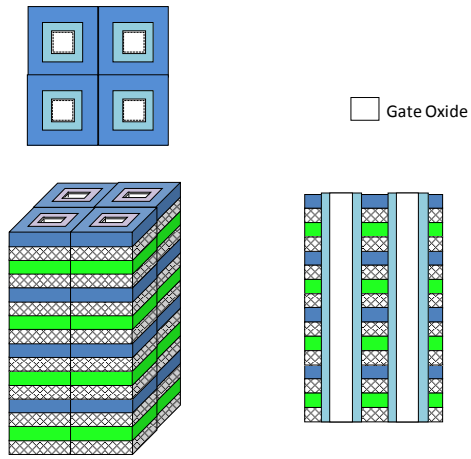

Figure 3 (F): Formation of gate oxide

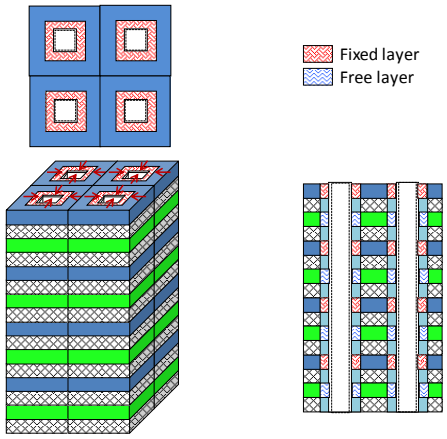

Figure 3 (G): Formation of fixed layer and free layer

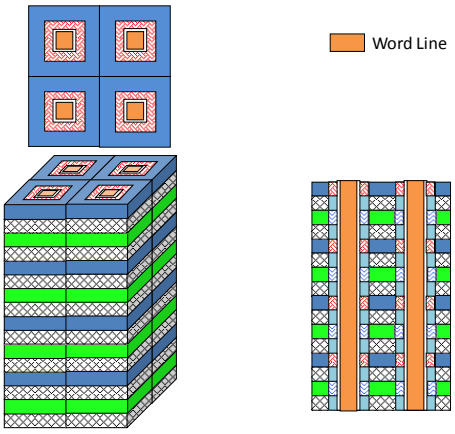

Figure 3 (H): Formation of WL

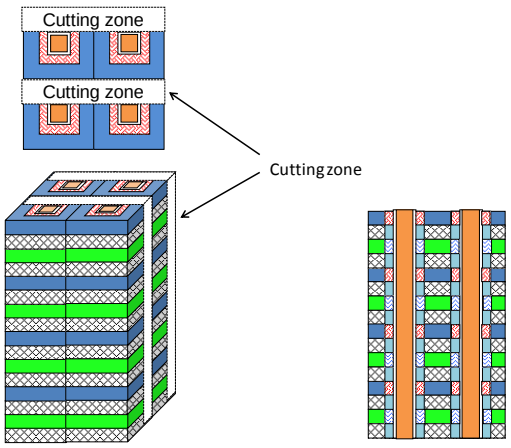

Figure 3 (I): Formation of trench between adjacent memory cell

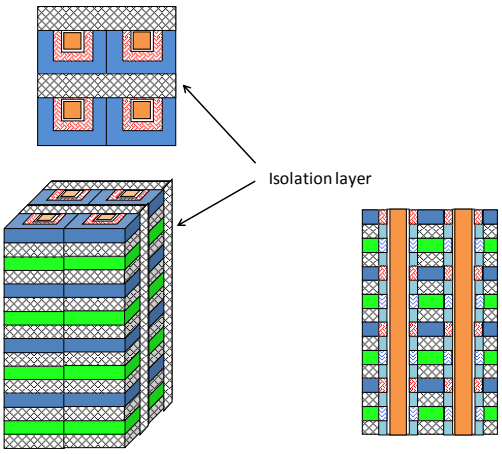

Figure 3 (J): Formation of isolation between adjacent memory cell

3 Analysis of bit cost of memory cell array for stacked type NOR MRAM

Bit cost of memory cell array for stacked type NOR MRAM is estimated using the process step shown in Fig.3. The estimated procedure is the same as that of stacked type NAND MRAM case [6] [9].

Estimated bit cost of memory cell array for stacked type NOR/NAND MRAM vs number of layer is shown in Fig.4. The yield of 1 layer NAND flash memory, Y=95%, is used as a parameter. Two process cases, process steps/layer of 0.04 for conventional process and 0.004 for ultra low process [6], are considered. Both structure memory cell size is the same value of $9F^2$.

There is an optimized bit cost for all cases. For all cases the optimized bit cost is very small compared with that with 1 layered NAND flash memory. This shows

that not only NAND structure but also NOR structure is promising candidate for realizing ultra low bit cost non-volatile memory.
For the same process/layer case, optimal bit cost for NOR structure is about two times larger than that with NAND structure. This is because the process steps/ layer for NOR case is two times larger than that for NAND case. For the further reduction of bit cost for NOR structure the reduction of process steps/layer and reduction of memory cell area are key issues.

	NAND		NOR	
process steps/layer	0.04	0.004	0.08	0.008
bit cost	0.2025	0.0206	0.4049	0.0412
optimized layer	64	512	32	256

Figure 4: Bit cost for cell array of stacked type NOR/NAND MRAM

4 Conclusion

In this paper the process step and analysis of bit cost of stacked type MRAM with NOR structured cell has been newly described. For NOR structure 4 layer process is needed for realizing 1 layer memory cell compared with 2 layer for NAND structure. Estimated bit cost for stacked type NOR MRAM is very small, 0.04-0.4, compared with that of 1 layered NAND flash memory. This shows that not only NAND structure but also NOR structure is promising candidate for realizing ultra low bit cost non-volatile memory. For the further reduction of bit cost for NOR structure the reduction of process steps/layer and reduction of memory cell area are key issues.

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