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An Optimized Direct Digital Frequency Synthesizer (DDFS)

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Abstract

An optimized Direct Digital Frequency Synthesizer (DDFS) design in terms of reduced ROM, high throughput and speed is designed in this paper. DDFS is designed with 200 MHz reference clock frequency and 32 bit FTW for the generation of sine and cosine signal with 16 bit output frequency having frequency resolution of 0.0466 Hz and Phase resolution of 0.0055°. DDFS design is simulated using VHDL in ModelSim 10.1d and then synthesized using Xilinx ISE 13.2 tool for implementation in FPGA-Spartan3E. The performance of designed Reduced ROM based DDFS shows that the latency of normal ROM based DDFS is improved by 369 ns. Through CORDIC algorithm, the Reduced DDFS is further improved by increasing its maximum frequency to 138.47 M Hz with latency of 73 ns and reducing its number of slices and LUTs by 56 %.

Keywords: DDFS, ROM, LUT, CORDIC Algorithm, FPGA Implementation

1 Introduction

Signal generators play a vital role in testing and debugging of various electronic systems by the generation of versatile waveforms which are necessary stimuli during testing [7]. Modern wireless communication system like spread spectrum technique requires signal with high frequency switching speed and better resolution compared to signals generated by conventional analog based Phase Locked Loop (PLL) [5] [6]. Moreover quadrature signals are necessary for digital modulation and for up down conversion. Such signal generation is possible through Direct Digital Frequency Synthesizers (DDFS) also called as Numeric Controlled Oscillator (NCO). DDFS generates a sine and cosine signal and it is capable of changing its output frequency by changing its reference clock frequency (F_{clk}) or tuning its frequency tuning word (FTW) also known frequency control word (FCW) since acting as a control signal [9].

An overview of DDFS is presented in next section. ROM based DDFS is presented in section 3 with normal and reduced approach. Section 4 deals with CORDIC algorithm approach. Implementations and experimental results are discussed and analysed in section 5 and concluded in section 6.

2 DDFS-An Overview

The simplified block diagram of DDFS is depicted in figure 1. The DDFS is consisting of a phase accumulator (PA), a sine/cosine generator, a digital to analog converter (DAC) and a filter [9].

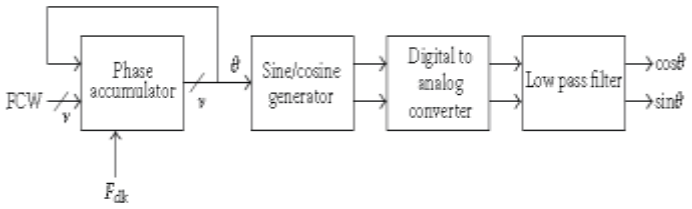

Figure 1: Simplified Block Diagram of DDFS

The phase accumulator increments FTW and its output represents phase information is given to sine/cosine generator which generates the discrete equivalent amplitude values form its incoming equivalent phase values. Then those values are converted to analog by passing it through a DAC and then to filter for continuous time sine/cosine generated signals as the generated outputs. The output frequency of DDFS is given by $F_{out} = \frac{FTW \ F_{clk}}{2^N}$ ----- (1) where

FTW is the frequency tuning word, F_{clk} is the clock frequency and N is the word length of the phase accumulator. The minimum and maximum frequency signal generated by DDFS can be calculated from the equation 2.

$$F_{min} = \frac{F_{clk}}{2^N} \ , \ F_{max} = \frac{F_{clk}}{2} \quad \text{----- (2)}$$

For a 200 MHz clock frequency and with 32 bit phase accumulator, a minimum frequency of 0.0466 Hz also known as frequency resolution and the maximum frequency of 100M Hz limited by Nyquist/Shannon sampling theorem is possible. From paper [5], FTW decides speed of rotation of phase wheel for generation of a full cycle of a sine/cosine wave. Thus higher speed enables high frequency wave generation. In conventional DDFS, the conversion from phase to amplitude is done through look up table (LUT).Increasing output width or the resolution of values in ROM for higher performance will demand a huge size which is not acceptable due to decrease in speed with increase in area and power dissipation [4] and requirement of high resolution DAC design. Therefore, there is a need to reduce the ROM size for better optimization of DDFS.

3 ROM based DDFS

In this approach, ROM acts as a LUT containing sin/cos values addressed by the phase information for conversion from phase to its equivalent amplitude values. The ROM is defined by 2^I x J, where I and J is the word length of input and output of the ROM. The phase accumulator N bits output can be truncated into M bits to reduce size of ROM. But this truncation will result in the phase truncation error which is acceptable against the ROM size reduction benefits [2] [3]. However M bits are not completely reducing the size of LUT.

3.1 Normal ROM based DDFS

In order to generate sine/cosine wave simultaneously from DDFS, there is a need of two ROMs of similar size of 2^I x J so that output wave will be in J no. of bits with resolution of 2^I. Its block diagram is shown in figure 2. For truncated M bit phase value, its equivalent P bits sine/cosine amplitude values are outputted by ROM static addressing.

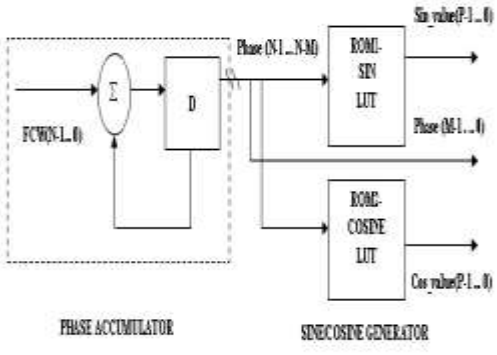

Figure 2: Normal ROM

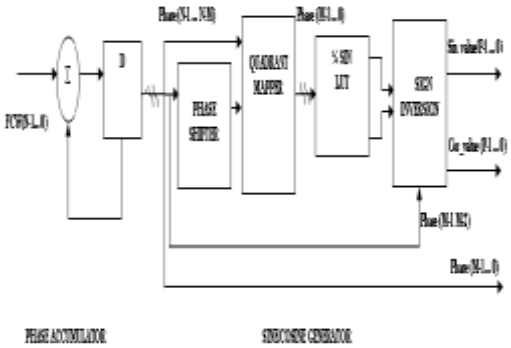

Figure 3: Reduced ROM

3.2 Reduced ROM based DDFS

The size of the ROM can be reduced by exploiting the trigonometric properties [1]. By using symmetric properties of sine wave where sin (pi+Θ) = -sin Θ, sin (pi-Θ) =sin Θ, etc., the size of ROM can be reduced from 2^I x J to 2^{I-2} x J. Compared to normal, reduced ROM based DDFS is still having two ROMs. The cosine ROM can be completely removed by using the phase shift property where sin (pi/2+Θ) = cos Θ. cos values can be found out from sine ROM by shifting the cosine angle by pi/2 and finding out sine values for the shifted angle. The reduced block diagram of normal ROM is shown in figure 3.

4 CORDIC based DDFS

Coordinate Rotation Digital Computer (CORDIC) uses less number of hardware such as shifters and adders/sub tractors for computing trigonometric functions. It rotates coordinate vector over unit circle through constant angles until the angle is reduces to zero. Volder's algorithm [10] derives rotated vector values by rotating the vector $[x_i, y_j]$ to $[x_{i+1}, y_{j+1}]$ from the general equations

$$x' = x\cos(\Theta) - y\sin(\Theta)\ ;\ y' = y\cos(\Theta) + x\sin(\Theta) \qquad \text{----- (3)}$$

Final output equations on n th iteration,

$$X_n = K[x_i \cos Z_i - y_i \sin Z_i];\ Yn = K[y_i \cos Z_i + x_i \sin Z_i] \qquad \text{----- (4)}$$

Where K =1.607253 after n =16 iterations. During an every iteration, comparison is made between the initial desired angle and the resulting angle and then based on the comparative result, sign is determined for the next rotation [8].

For the generation of sine/cos wave by CORDIC based approach, phase accumulator output is initialized as the desired rotation angle along with initial x and y values as 1/K and 0 respectively, are given to CORDIC block. Since CORDIC algorithm converges around –pi/2 to pi/2, the two MSB bits of phase accumulator is used to generate wave for a complete cycle of period 0 to 2pi by quadrant mapping and sign inversion for the desired angle values at the appropriate quadrants is need to done as given in figure 4.

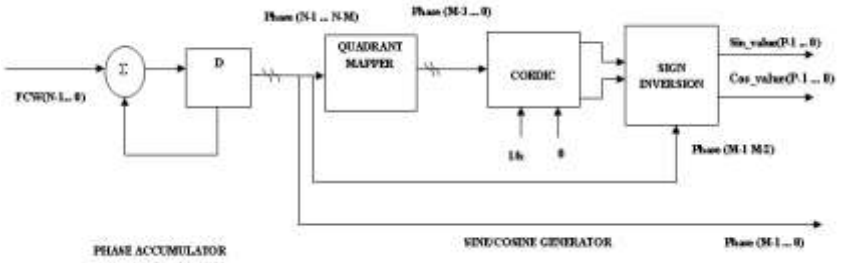

Figure 4: Block Diagram of CORDIC based DDFS

5 Implementation and experimental results

Simulations are done with FTW of 32 bits and clock frequency of 200M Hz by changing the phase width of wave with an amplitude width of 12 and 16 bits each. For an output frequency of 10 M Hz and 5 MHz, FTW of 214748364 and 107374182 has to be given which can be calculated from the equation 1.It is observed that the output wave frequency is changed from one to other as soon as FTW is changed as shown in figure 6. The designed architecture can be implemented in FPGA using the VHDL language and synthesized using XILINX ISE 13.2 tool for the target device of Spartan 3E FPGA.

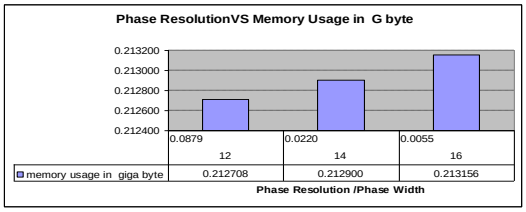

Figure 5: resolution vs memory usage

	Maximum Frequency in MHz	Number of slices	Number of 4 Input LUTs
Reduced ROM based DDFS	67.788	799	1516
Pipelined CORDIC based DDFS	138.466	450	848

Table 1: Performance of DDFS.

The performance of ROM based DDFS can be analysed from the maximum output required time after clock which is 6.492ns for normal ROM and 6.123 ns for reduced ROM. Thus latency is improved by 369 ns. Higher the phase width, higher the area which can be observed through increase in memory usage with an advantage of the increase in output resolution from the figure 5.

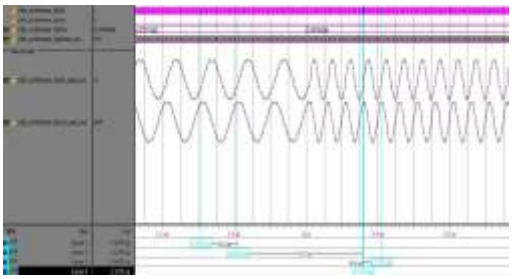

Figure 6: Reduced Based DDFS

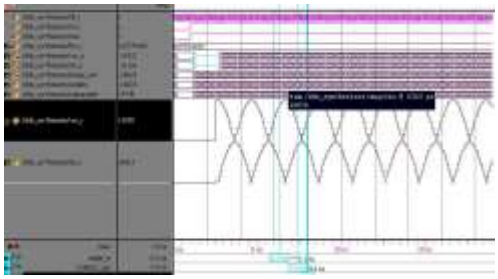

Figure 7: CORDIC Based DDFS

For further improvement in the performance, pipelined CORDIC algorithm is developed in VHDL. For 16 bit input angle of 108° = 19660, CORDIC block gives sin 108° and cos 180° with frequency resolution 0.04657Hz and Phase resolution is 0.0055°. Since ROC of CORDIC is ± 90°, angle is mapped to 13104 (72°) and CORDIC block gives outputs for sin and cos angle as 31166 and 10122 respectively. But cos 108° needs negative sign which is done in sign converter and its outputs are 31166 and -10122 respectively as DDFS outputs. Compare to other technique, the speed is increased with maximum frequency of 138.47MHz and also the number of slices and LUTs are reduced as shown in table 1.

6 Conclusions

This paper shows that compared to normal ROM based DDFS, reduced ROM based DDFS is good by taking an advantage of trigonometric properties but CORDIC algorithm is further improving its performances through high throughput. The designed reduced ROM decreases the system latency of the normal ROM by 369 ns and CORDIC based DDFS is further reducing the number of slices and LUTs of reduced ROM based DDFS with latency of 73 ns and maximum frequency of 138.47 M Hz. Thus proposed DDFS is optimized in terms of speed even though it uses the same phase accumulator for both methods with larger size for higher resolution. Such results will be further improved for better output frequency provided pipelined scale free CORDIC algorithm is used and implemented for ASIC synthesis. The future work will be subjected to ASIC synthesis such that power estimation can be made and applying DDFS in spread spectrum communications system.

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