Comparison of Various Optimized Architectures

of DCO for ADPLL

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Abstract

Digitally controlled oscillator (DCO) form the core of all digital phase locked loop (ADPLL).Nowadays portable batteries play a vital role in communication systems, hence low power circuits with reduced hardware are important. These criterions are satisfied by the proposed architecture. Different DCO designs with 3T NAND and 3T NOR gates as inverters proposed along with the result of 3T XOR and 3T XNOR gates are compared.XOR based digitally controlled ring structure produces the frequency of [2.93 to 3.80 GHz] with power consumption of [293 to 369 µW] where as XNOR design produces [1.35 to 1.64 GHz] with power consumption of [195 to 223 µW]. The reported designs of NAND and NOR produces a frequency of [3.11 to 3.97 GHz] and [5.80 to 6.24 GHz] with power consumption of [293 to 369µW] and [841 to 858 µW] respectively. In this paper the proposed designs shows improvement in performance over the existing designs.

Keywords: DCO, ADPLL, ring structure,3 transistor structures, power consumption

1. Introduction

While CMOS technologies are growing exponentially, there is high necessity for high speed and minimal power components. Most of the electronic circuits require faster clock generation[1][3]. To achieve faster clock generation faster locking PLL (Phase Locked Loop) is required. Controlled oscillators from the core of a PLL, Nowadays there is transition from analog controlled oscillators to digitally controlled structures since the performance of analog controlled oscillators is influenced by process parameters and noise. Digitally controlled oscillators overcome the limitations of analog components with convincing performance. Digital circuits have the merits of robustness; higher noise immunity and fast acquisition, while a single concern have upper hand over all the merit of a DCO. Digitally controlled oscillators consume nearly half of the total power consumed by a phase locked loop[10]. Some process requires ADPLL (All Digital PLL) which generates fewer frequency components, on such systems lower pulling range is acceptable.
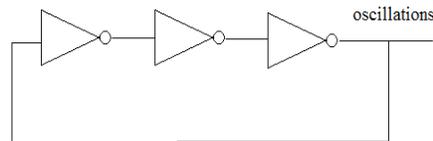
Figure 1: Ring Oscillator.

The inverters shown in the figure 1 are replaced by 3T XOR, XNOR, NAND and NOR gates for producing oscillations which are discussed in Section 2 and 3.

2. Existing method

DCO structures that makes use of 3T XOR[7] and 3T XNOR cells as inverters are explained. Delay adjusted through digital bits is used since digital controls provide high noise immunity and better tune ability[9]. When VDD is fixed at one of the inputs an XOR gate performs inversion while one terminal of XNOR gate is fixed,it performs inversion. By eliminating a direct path from VDD to ground, short circuit current can be reduced to a negligible value and also the structures produce a small switching activity hence the power consumption[4] is reduced to a higher extent. The XOR based inverter is designed with having every such criterion in mind. Delay elements form the core of a DCO and require special care NMOS switch networks[6] are used throughout this paper. Binary weighted NMOS transistors have varying widths are used in order to obtain various frequency. The inverters structures of 3T XOR and 3T XNOR with NMOS switching network are shown in figure 2a and

figure 3a and their corresponding oscillator output was shown in figure 2b and figure 3b.
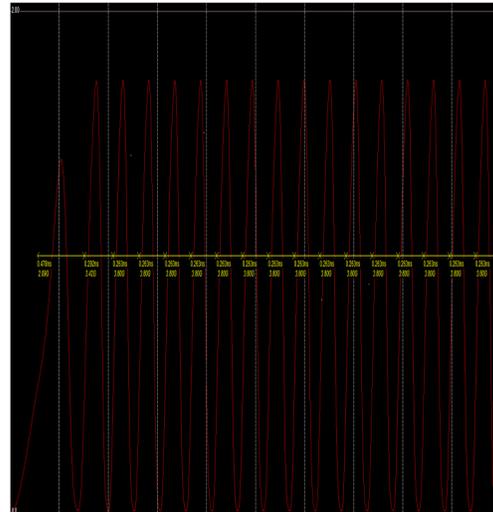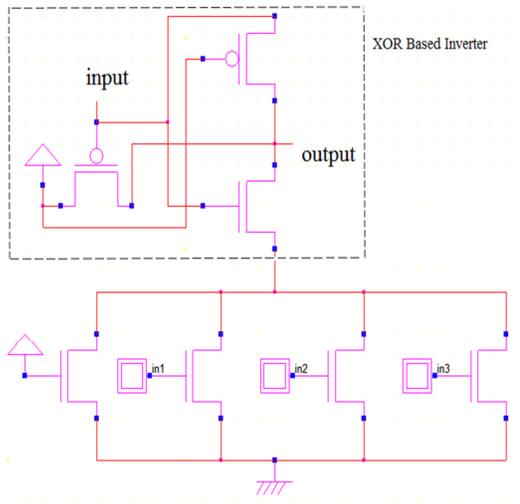

Figure 2a: XOR based inverter.
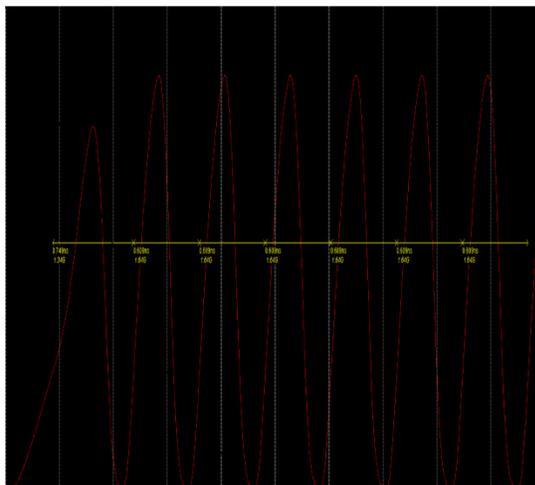

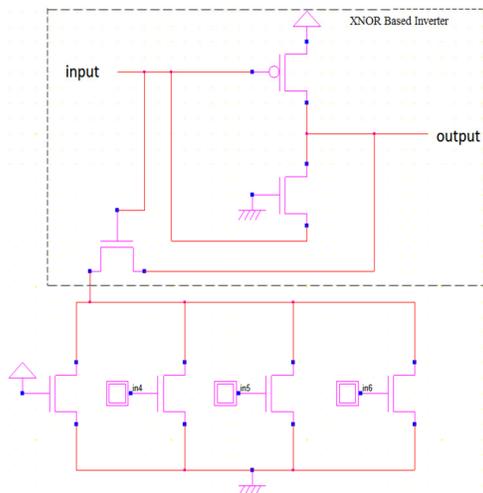**Figure 2b:** XOR based oscillator output.

Figure 3a: XNOR based inverter.

Figure 3b: XNOR based oscillator output.

3. Proposed system

DCO structures that makes use of 3 transistors NAND and NOR gate are used which can also produce inversion while one terminal is converted to VDD and ground respectively. Both are universal gates and produce faster switching when compared to former design. NMOS delay network is used for producing different frequency components whereas the same can be replaced by PMOS switching network which can attain much more reduced power with the demerits of lesser frequency. The system will produce frequency of around 3 to 4 GHz, which can be used for PLL in Bluetooth applications. The inverters are connected in a closed feedback loop and the numbers of inverting stages should be odd. Hence three stage ring oscillator structure is used. For higher tuning range the number of inverting stages can be increased. For fine tune ability the number of transistor in the switching network should be increased. The width of NMOS transistors in the delay cell should be[7],

$$N_n = 2^{n-2} \times 0.5 \ \mu m.$$

Hence the width of N_1, N_2, N_3 and N_4 is 0.5µm, 1µm, 2µm and 4µm respectively.
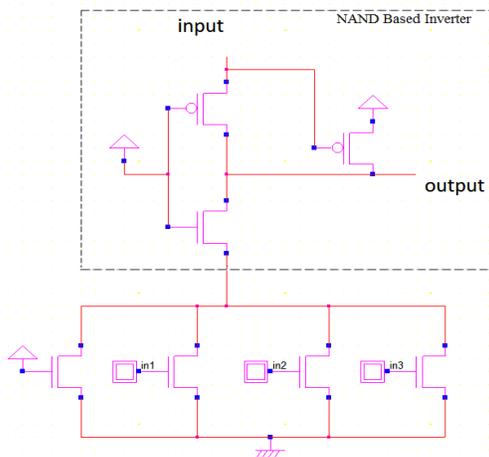

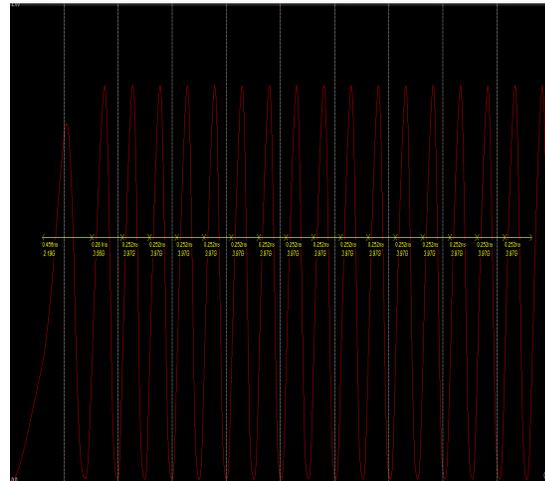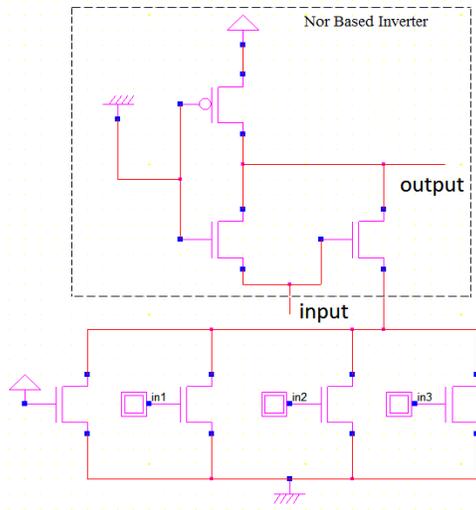**Figure 4a:** NAND based inverter.   **Figure 4b:** NAND based inverter.
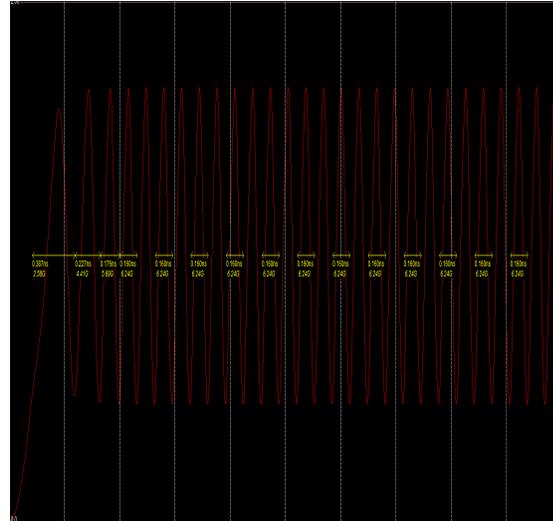
Figure 5a: NOR based inverter.

Figure 5b: NOR based inverter.

4. Results and discussion

The results are obtained using Microwind 3.1 layout generator in 0.18 micro meter technology. The graph shows the comparison between all four structures and the comparison table explains the frequency and consumed power for each structure to its corresponding control bits [000-111].

4.1 Comparison:

CONTROL BITS	XOR		XNOR		NAND		NOR	
	FREQUENCY (GHz)	POWER (µW)	FREQUENCY (GHz)	POWER (µW)	FREQUENCY (GHz)	POWER (µW)	FREQUENCY (GHz)	POWER (µW)
000	2.93	293	1.35	193	3.11	294	5.80	841
001	3.74	365	1.62	224	3.91	365	6.21	854
010	3.63	356	1.59	220	3.80	355	6.16	857
011	3.79	368	1.63	224	3.96	368	6.23	852
100	3.47	343	1.55	215	3.64	343	6.12	850
101	3.77	366	1.63	224	3.94	366	6.22	856
110	3.70	361	1.61	223	3.87	361	6.19	853
111	3.80	369	1.64	225	3.97	369	6.24	858

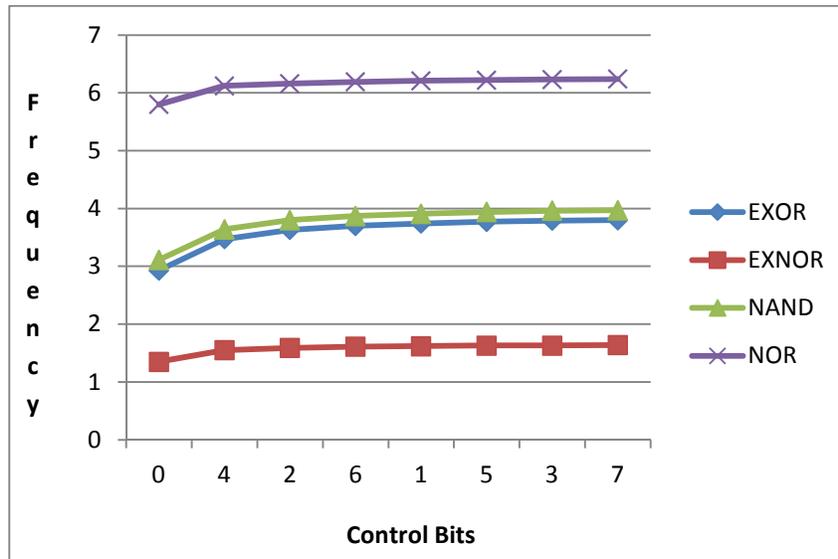**Table 1:** Comparison of frequency and power of DCO structures.

Figure 6: Graphical representation of DCO frequencies.

5. Conclusion and Future work

The proposed structures produce a higher frequency when compared to the existing XOR and XNOR structures. NAND produces a higher frequency of [3.11 to 3.97 GHz] with the same power consumption [2.94 to 3.69 µW] to that of XOR architecture which produces the frequency of [2.93 to 3.80 GHz]. NOR architecture produces a higher frequency [5.80 to 6.24 GHz] but consumes more power nearly thrice the power consumed by NAND architecture. Hence NAND based oscillator design can be used for Phase Locked Loop in portable devices due to its low power consumption where as NOR based oscillators design can be used for high frequency applications. PLL can be designed with 3T NAND and 3T NOR architecture for Bluetooth applications in future.

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