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A Systematic Eight Port Network on Chip Router with Reduced Critical Section Problem

T. Saipriyadharshini and R. Parameshwaran

SASTRA University, India

Abstract

Network on chip is an emerging technology which provides data reliability and high speed with less power consumption. The central component of NOC architecture is a router that should be designed in an efficient manner. In NoC designs, parallel transfers of data between the PEs are possible. This flexibility comes at the cost of additional area and power dissipation. The proposed work consists of an eight port router with high speed which provide high throughput and with less latency. In arbiter the Round Robin algorithm is implemented as binary semaphore to avoid the critical section problem. Router design is simulated using Verilog HDL in Modelsim 6.5b software and it is synthesized in a Xilinx ISE 14.2.

Keywords: NoC, central component, router, eight port router, round robin, semaphore, critical section problem

1. Introduction

The approach of Multi-processor system on chip is the rising edge technology for System on chip design (SOC). The designing of wire and power consists of many constraints pushing towards the new designing methodologies [12]. General problem in SOC can be elaborated in terms of power, size and performance metrics. In practical multi-processor chips consists of single bus interconnection. Shared bus designs are efficient but it has an underlying limitations. Solution for this problem is Network on Chip (NoC) [6]. Network on chip architecture better supports the integration of SOC which consists of on chip packet switched network. Bandwidth requirement can be satisfied by using on-

chip packet-switched network of interconnects, known as NoC architecture [10]. Idea behind this is comes from large-scale multi-processors and distributed computing networks [3]. In general network on chip routers are implemented in FPGAs (Field Programmable Gated Arrays). So that the fabrication process cost using this kind of FPGA is an essential one. It is estimated by the ratio between wires and transistors. FPGAs are capable to provide flexibility and statistically routed bit-based wiring. This flexibility can be obtained by using high area, latency and power [4] [7].

The prior work has been done with five port and eight port router. But the critical section problem was not taken for consideration. In proposed work eight port router is implemented with reduced critical section problem.

2. Eight port router

Design of NoC router consists of Packet format, arbiter design, cross bar and queue design. It can be designed in any of the two forms depending upon the usage such as five port router and eight port router[5] [6] . In 8 port router it deals North(N), East(E), West(W), South(S), North-East(NE), North-West(NW), South-West(SW) and the remaining one port is connected with processing element(PE). Here the port can be shared in 2 directions. Such as South-West, it deals with both directions [8]. Routing process affords high speed. Compared to five port, 8 port consumes little more area but it provides high speed and through-put. Hence the additional area usage can be justified with its speed. Here the implementation is deals with 8 port hard router which provides high speed. This is implemented in 2D (2-Dimensional) such as X axis and Y axis.

3. Packet format

Main issue in the on-chip router is the design of packet format [5]. Total packet size is 160 bits. In these 160 bits, destination and source address is assigned for the first 6 bits. First 3 bits pointing the destination address and the succeeding 3 bits for source address. Leftover 154 bits assigned for the original data bits. The proposed packet format is shown in the figure 1.

Figure 1: Packet format

4. Eight port router arbiter

To resolves the contention problem and the control towards the arbitration of the ports, router needs an arbiter [5]. It consist the status of all the input, output ports and keeps tracking that which port is free and which is having intercommunication with other port. Once the port is fixed for the work it is

connected to the crossbar. Output port is reserved for the input port until the transmission gets finished [9] [11]. In proposed work, arbiter is implemented in the form of semaphore. Semaphore is a methodology which can allow a particular task can to do its work in a particular time. By this approach critical section problem can be avoided. This is a binary semaphore and it has only two possibilities such as 0 and 1.

The credit is taken as a semaphore element. If the credit is 1, it indicates that particular port is busy i.e., some other port is using this current port. Hence the transfer cannot be taken place. On the other hand if the credit is 0 then the particular port is free. The transfer of packet can be accomplished through this particular port. Pseudo code is shown in figure 2. Both credit and grant are control signals. This semaphore is achieved using round robin process scheduler algorithm [1]. Packets can be transferred according to its time quantum which is a predefined one. This time quantum is established in the form of number of clock cycles. For a single transfer it has been set as 4 clock cycle that is for every four clock cycle, packet will be transferred.

```
if (credit==1) // port is busy
wait
if (credit==0) // port is free
if(credit==0)
grant=1;
else
grant=0;
```

5. Cross-bar for eight port router

A cross-bar switch is also known as matrix switch or cross-point switch. A connection between multiple inputs to multiple outputs is established through the cross-bar in a matrix manner [1]. This cross-bar switch consists of 8 inputs and 8 outputs. Depending upon the control signal (also known as select signal) generated by arbiter, the connection distribution between input port and output port is established through cross-bar switch. Simple cross-bar switch is implemented using multiplexers. Inside the cross-bar according to the router size multiplexer size gets varying. For 8 port router 8:1 multiplexer is used. Control line is checked with predefined 3 bits. Output of the 8X8 router is an output of multiplexers [2] [5] [6]. The source and destination address along with first six bits of data is shown in table 1.

6. Queue concept in eight port router

A Queue is a data structure concept which is used to arrange the data in a First In First Out manner [2]. FIFO is used as temporary buffer. In queuing system the data-network is a one where packets arrive, wait in various queues, receive service at various points, and exit after some time. In both input port and output port, separately FIFO block is designed. The work done by FIFO block is to route the packet which come first and has to wait until it gets routed. Then it should allow the next packet to get transfer [5]. Two main operation of this FIFO block is as follows [3]: Write operation and Read operation

This block designed with the capacity to handle particular number of bits. The operation permitted to use these bits alone. If it has crossed the limits, any of the following 2 states may occur. Data underflow and data overflow. Data underflow is the state when the data is not presents in the buffer, still approaches with read operation. Likewise data overflow state is the state when the buffer is already exhausted but trying to write any new data. Both states can never occur. Here the FIFO buffer is implemented using queue concept for the 8 port router.

Ports	First six bits of packet	Source Address	Destination Address
Port a	$(000001)_2$ $(1)_{16}$	000	001
Port b	$(001010)_2$ $(A)_{16}$	001	010
Port c	$(010011)_2$ $(13)_{16}$	010	011
Port d	$(011100)_2$ $(1C)_{16}$	011	100
Port e	$(100101)_2$ $(25)_{16}$	100	101
Port f	$(101110)_2$ $(2E)_{16}$	101	110
Port g	$(110111)_2$ $(37)_{16}$	110	111
Port h	$(111000)_2$ $(38)_{16}$	111	000

Table 1: First six bit packet and source and destination address

7. Result analysis

7.1 Simulation

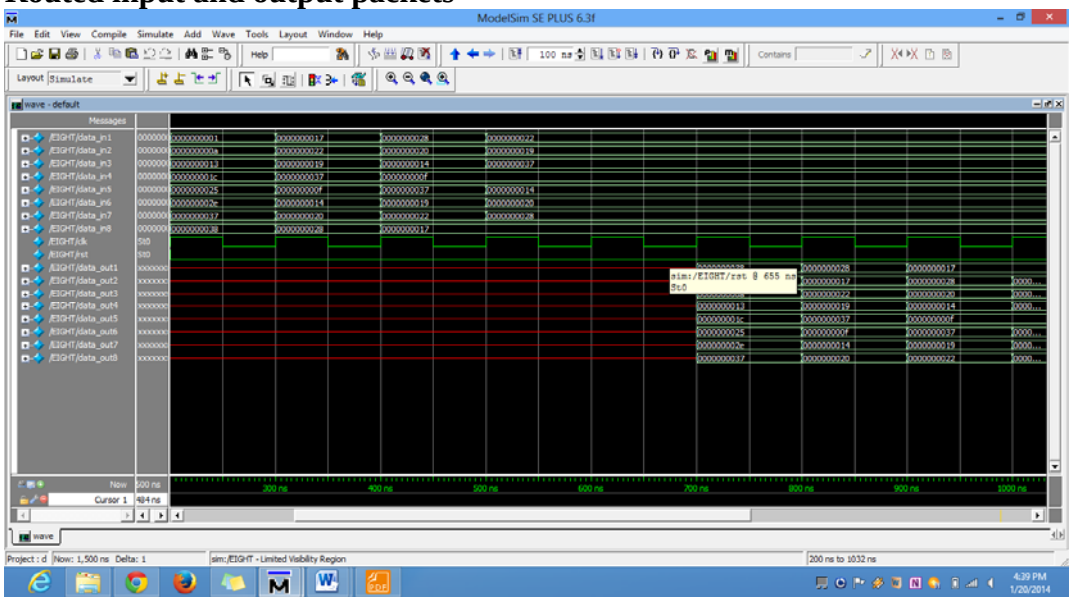
ModelSim 6.5b is used for simulation. Port is assigned with particular source and destination address. After four clock cycle port transmit that particular packet to the destination port.

7.2 Synthesis

Synthesis is done in Xilinx ISE 14.2 tool.
This synthesis report is verified in FPGA-XILINX (DEVICE SELECTED – 3S500EFG320-4) Speed Grade: -4
Minimum period: 50.715ns (Maximum Frequency: 19.718MHz)
Minimum input arrival time before clock: 51.589ns
Maximum output required time after clock: 6.168ns
Maximum combinational path delay: No path found

7.3 Simulation result 1

Routed input and output packets



8. Conclusion and future work

The proposed router is significantly increases the throughput. Input data of the router can be varying from 0 to 160 bits. Port address is assigned by the shortest distance between the input port and the output port. If priority is assigned by checking the length of packet it will leads to a problem of starvation. Because the longer data gets the highest priority, so routing operation takes place for the entire longest data packet in worst case. Hence the smallest length data packet has to wait for long time to get routed. This designed eight port router provides high speed in a network. Comparing to five port router this eight port router can route the data in less hop count. In this the arbiter scheduling can be improved by assigning priority in the form of fair-share scheduling.

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