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Circuit Design of 2-Input Reconfigurable Dynamic Logic Based on Double Gate MOSFETs with Whole Set of 16 Functions

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Abstract

Circuit design of 2-input reconfigurable dynamic logic based on double gate MOSFETs with the whole set of 16 functions has been newly described. 16 function 12T DRDLC with two states (+V, 0) of control gate voltages and 14T DRDLC with two states (0, -V) of control gate voltages have been newly proposed. From these two states control gate case, 12T DRDLC with three states (+V, 0, -V) of control gate voltages is successfully derived. Newly proposed DG-MOSFET with two states (+V, 0), (0, -V) cases can be successfully realized using presently available OR type, AND type IDG-MOSFET, respectively. Newly proposed circuit design, especially for 16 functions 12T DRDLC with two states (+V, 0) case is the promising candidates for realizing future reconfigurable LSIs.

Keywords: reconfigurable logic, double gate MOSFET, FinFET

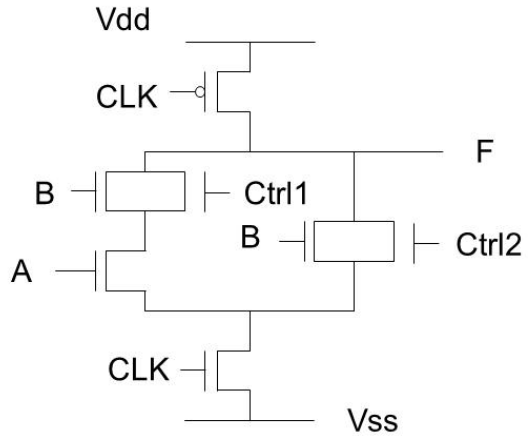
1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem various kinds of 3D transistors has been proposed. FinFET [2][3] which use the 3 planes as the channel for reducing the short channel effect has been developed. The application of FinFET which uses the same input for both sidewall channel to high end MPU begins[4][5]. This is because the fabrication technology of FinFET is almost the same as that of the presently available conventional planar transistor except for the trench isolation for transistor formation.
On the other hand for reducing the number of transistors for logic circuit Independent-gate controlled Double Gate transistor, DG transistor, has been proposed[6]. Independent-gate controlled Double Gate transistor uses the sidewall as the channel with using two independent input signal. Therefore, two conventional planar transistors connected in series or parallel can be reduced to one Independent-gate controlled Double Gate transistor by controlling device parameters such as the impurity concentration of body or gate oxide thickness[7].
Various kinds of logic circuit is designed using this structure[8][9]. Independent-gate controlled Double Gate transistor is promising candidate for the next generation of FinFET.
Furthermore, by using first gate for input signal and second gate for control signal Independent-gate controlled Double Gate transistor (DG MOS FET) can be used for the dynamic reconfigurable logic. First report for this application was 2-input dynamically reconfigurable dynamic logic circuit (DRDLC) with 5 transistors using three states (+V, 0, -V) of the control gate voltages[10]. Using this circuit 4 logic functions can be realized. However, this value of 4 is too small compared to 2^4=16 which is required for two Boolean input circuit. DRDLC which generate the whole set of 16 functions has not been reported. Second and third reports describes only the combination with CNTFET[11] and pattern design[12].
In this paper circuit design of DRDLC with two Boolean inputs focusing on the generation of whole set of 16 functions has been newly described.
This paper is organized as follows. In section 2 new type DRDLC with only 12 transistors using two states (+V, 0) of control gate voltages and new type DRDLC with 14 transistors using two states (0, -V) of control gate voltages has been proposed. In section 3, DRDLC with 12 transistors using three states (+V, 0, -V) of control gate voltages is derived from the newly proposed circuit described in section 2. In section 4 the relation between the newly proposed circuit described in section 2/3 and the previously proposed Independent-gate controlled Double Gate transistor of ref[6]-[9] has been described. Finally, a conclusion of this work is provided in Section 5.

2 Newly proposed 16 function 12-14T DRDLC using two states of control gate voltages

In section 2, firstly, 4 function DRDLC with 5 transistors using three states (+V, 0 , -V) of the control gate voltages[10] has been described. After that, new type DRDLC with only 12 transistors using two states (+V, 0) of control gate voltages and new type DRDLC with 14 transistors using two states (0, -V) of control gate voltages have been proposed.

Conventional 4 function DRDLC with 5 transistors using three states (+V, 0, -V) of the control gate voltages[10] is shown in Fig.1(A). This circuit has two Boolean data inputs (A and B), two configuration inputs (Ctrl1, Ctrl2), and clock input (CLK) and one output of F. In this figure, each transistor consists of a DG-MOSFET and configuration inputs (Ctrl 1, Ctr2) have three states (+V, 0, -V) of signal gate voltages. These configuration input control DG-MOSFET as on-state for +V (Vdd), N-type configuration for 0, and the off-state for –V as shown in Fig.2. Clock inputs (CLK) has the role of the dynamic logic style[13] used in this circuit. Finally, the output of circuit F is decided as 0 and plus voltage corresponding “1” by Boolean inputs A and B. In this way, configuration inputs (Ctrl1, Ctrl2) determine the logic function realized by the circuit in Fig.1(A). Fig.1(B) shows the configuration inputs and the corresponding logic function of F.



(A)

Ctrl1	Ctrl2	F
0	-V	$\overline{A \times B}$
Vdd	0	$\overline{A + B}$
Vdd	-V	$\overline{A}$
0	0	$\overline{B}$

(B)

Figure 1: Conventional 4-function 5T DRDLC with three state (+V, 0, -V).
(A) Circuit diagram, (B) Configuration inputs and corresponding logic functions.

4 functions can be successfully realized with only 5 transistors. However, this conventional DRDLC can realize only 4 functions which are too small compared to whole set of 16 functions. Therefore, the conventional DRDLC can be used to the limited application. Furthermore, conventional DRDLC operates using three states (+V, 0, -V) of the control gate voltages. Conventional Independent-gate controlled Double Gate transistor (DG FET) operates using two states such as (+V, 0) of the control gate voltage[6]-[9]. Therefore, for realizing three states (+V, 0, -V) of the control gate voltages extra process technology should be introduced. In order to overcome these problem about the limited application and extra process technology 12-14T DRDLC which can generate 16 functions with two states of the control gate voltages have been newly proposed.

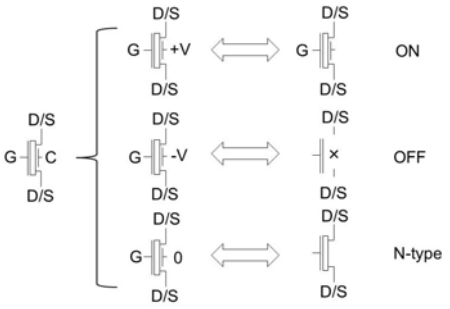


Figure 2: DG-MOSFET device symbol and configurations with three state (+V, 0, -V).

Newly proposed 16 function 12T DRDLC is shown in Fig.3. This circuit consists with 12 transistors using two states (+V, 0), six configuration inputs (C1-C6), and two clock inputs (CLK, /CLK). Table 1 shows the configuration inputs and the corresponding inputs and corresponding logic function of $\overline{Y}$.

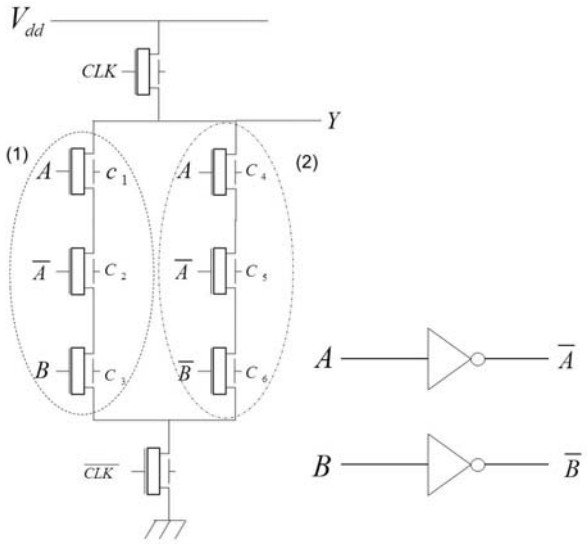


Figure 3: Newly proposed 16-function 12T DRDLC with two states (+V, 0).

Table 1: Configuration inputs and corresponding logic functions for newly proposed 16-function 12T DRDLC with two state (+V, 0).

C_1	C_2	C_3	C_4	C_5	C_6	$\overline{Y}$
0	**+V**	**0**	**0**	**0**	**+V**	AB
+V	**0**	**0**	**0**	**0**	**+V**	$\overline{A}B$
0	**0**	**+V**	**0**	**+V**	**0**	$A\overline{B}$
0	**0**	**+V**	**+V**	**0**	**0**	$\overline{A}\overline{B}$
+V	**0**	**0**	**0**	**+V**	**0**	$A \oplus B$
0	**+V**	**0**	**+V**	**0**	**0**	$\overline{A \oplus B}$
0	**+V**	**0**	**0**	**+V**	**0**	A
+V	**0**	**0**	**+V**	**0**	**0**	$\overline{A}$
+V	**+V**	**0**	**0**	**0**	**+V**	B
0	**0**	**+V**	**+V**	**+V**	**0**	$\overline{B}$
+V	**+V**	**0**	**0**	**+V**	**+V**	$A + B$
+V	**+V**	**0**	**+V**	**0**	**+V**	$\overline{A} + B$
0	**+V**	**+V**	**+V**	**+V**	**0**	$A + \overline{B}$
+V	**0**	**+V**	**+V**	**+V**	**0**	$\overline{A} + \overline{B}$
+V	**+V**	**+V**	**+V**	**+V**	**+V**	T
0	**0**	**+V**	**0**	**0**	**+V**	$\perp$

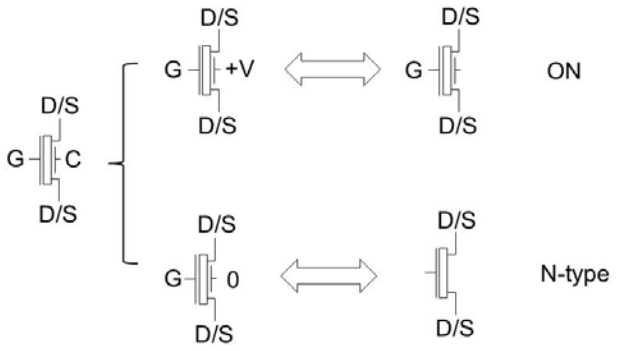


Figure 4: DG-MOSFET device symbol and configurations with two state (+V, 0) used in Fig.3.

For realizing two states of the control gate voltages, there are two candidates. They are (+V, 0) scheme or (0, -V) scheme. Fig.3 uses (+V, 0) scheme. The configuration input control DG-MOSFET as on-state for +V, N-type configuration

for 0 as shown in Fig.4. For realizing 16 functions $A, B, \overline{A}, \overline{B}$, off-state and on-state must be realized with one DG-MOSFET or with block of DG-MOSFET. For DG-MOSFET case the invert signal of input, $\overline{A}$ and $\overline{B}$ can not be generated using one DG-MOSFET. Therefore, using the inverter circuit $\overline{A}$ and $\overline{B}$ are generated as shown in Fig.3. For (+V, 0) case, on-state can be realized using one DG-MOSFET. However, off-state can not be realized using one DG-MOSFET. Therefore, using logic $A \cdot \overline{A} = 0$, off-state is realized. For this purpose three DG-MOSFETs connected in series, input to gates are A and $\overline{A}$, are employed. Furthermore, for realizing the most complex logic, XOR and XNOR, complex circuit must be introduced[14]. For this purpose, two circuit blocks (1),(2) must be connected in parallel as shown in Fig.3. Each circuit block is consisted with three DG-MOSFET connected in series, input gate are A or $\overline{A}$ and (B or $\overline{B}$). The circuit of Fig.3 satisfied these requirements. By using the circuit shown in Fig.3 16 functions can be successfully generated as follows.

For realizing 3 logics about B,($AB, \overline{A}B, B$), circuit block (1) is activated using the voltage of control gates as shown in Table 1. In this situation circuit block (2) is set to off-state using C4=C5=0.

For realizing 3 logics about $\overline{B}$,($A\overline{B}, \overline{A}\overline{B}, \overline{B}$), circuit block (2) is activated using the voltage of control gates as shown in Table 1. In this situation circuit block (1) is set to off-state using C1=C2=0.

For realizing XOR and XNOR both circuit block (1) and (2) are activated.

For realizing A or $\overline{A}$, both (1) and (2) are activated. And also logic of $B + \overline{B} = 1$ is used for the signal of B or $\overline{B}$.

And also for realizing $A + B$, $\overline{A} + B$, $A + \overline{B}$ and $\overline{A} + \overline{B}$, both circuit block (1) and (2) are activated using the voltage of control gate as shown in Table 1.

For realizing 0, both circuit block (1) and (2) are set to off-state by using C1=C2=C4=C5=0.

For realizing 1, both circuit block (1) and (2) are set to on-state by using C1=C2=C3=C4=C5=C6=+V.

Using the circuit shown in Fig.3 16 functions can be realized using only 12 DG-MOSFET.

As previously described, for realizing two states of the control gate voltages, there are two candidates. They are (+V, 0) scheme or (0, -V) scheme. Fig.3 uses (+V, 0) scheme. Using (+V, 0) 16-function 12T DRDLC can be successfully realized. Another scheme, (0, -V) scheme leads to the 16-function 14T DRDLC as shown in Fig.5. This circuit consists with 14 DG-MOSFET using two states (0, -V), eight configuration inputs (C1-C8), and two clock inputs (CLK, /CLK). Table 2 shows the configuration inputs and the corresponding inputs and corresponding logic function of $\overline{Y}$. The configuration input control DG-MOSFET as N-type configuration for 0, off-states configuration for –V as shown in Fig.6.

For DG-MOSFET case the invert signal of input, $\overline{A}$ and $\overline{B}$ can not be generated using one DG-MOSFET. Therefore, using the inverter circuit $\overline{A}$ and $\overline{B}$ are generated as shown in Fig.5 as the same as Fig.3. For (0, -V) case, off-state can be realized using one DG-MOSFET. However, on-state can not be realized using one DG-MOSFET. Therefore, using logic $A+\overline{A}=1$, on-state is realized. For this purpose two DG-MOSFETs connected in parallel, input to gates are A and $\overline{A}$ or B and $\overline{B}$, are

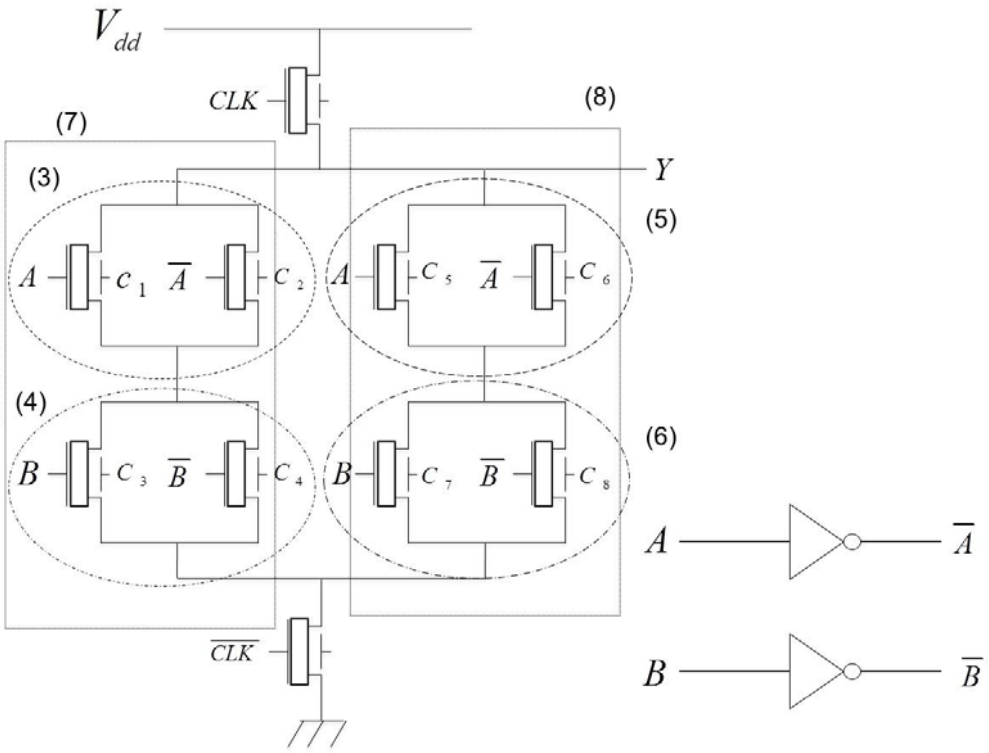


Figure 5: Newly proposed 16-function 14T DRDLC with two states (0, -V).

Table 2: Configuration inputs and corresponding logic functions for newly proposed 16-function 14T DRDLC with two state (0, -V).

C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	$\overline{Y}$
0	-V	0	-V	-V	-V	0	0	AB
-V	0	-V	0	-V	-V	0	0	$\overline{A}B$
-V	-V	-V	-V	0	-V	-V	0	$A\overline{B}$
-V	-V	-V	-V	-V	0	-V	0	$\overline{A}\overline{B}$
-V	0	0	-V	0	-V	-V	0	$A \oplus B$
-V	0	-V	0	0	-V	0	-V	$\overline{A \oplus B}$
0	-V	0	-V	0	-V	-V	0	A
-V	0	0	-V	-V	0	-V	0	$\overline{A}$
0	0	0	-V	-V	-V	-V	-V	B
-V	-V	-V	-V	0	0	-V	0	$\overline{B}$
0	-V	0	0	0	0	0	-V	$A + B$
-V	0	0	0	0	0	0	-V	$\overline{A} + B$
0	-V	0	0	0	0	-V	0	$A + \overline{B}$
-V	0	0	0	0	0	-V	0	$\overline{A} + \overline{B}$
0	0	0	0	0	0	0	0	T
-V	-V	-V	-V	-V	-V	-V	-V	$\perp$

employed. This two DG-MOSFETs connected in parallel is a smallest circuit block. Furthermore, for realizing the most complex logic, XOR and XNOR, four smallest circuit blocks (3)-(6) are connected as the same as Fig.3. The circuit of Fig.5 satisfied these requirements.

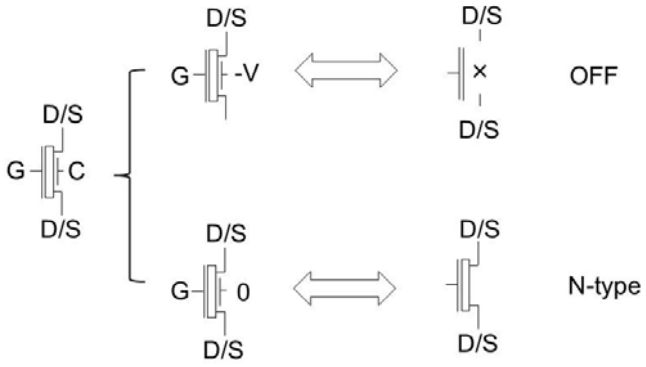


Figure 6: DG-MOSFET device symbol and configurations with two state (0, -V) used in Fig.5.

16 functions can be successfully generated as follows.

For realizing 3 logics about B, (AB, $\overline{A}B$, B), circuit block (7) is activated using the voltage of control gates as shown in Table 2. In this situation circuit block (8) is set to off-state using C5=C6=-V.

For realizing 3 logics about $\overline{B}$, ($A\overline{B}$, $\overline{A}\overline{B}$, $\overline{B}$), circuit block (8) is activated using the voltage of control gates as shown in Table 2. In this situation circuit block (7) is set to off-state using C1=C2=-V.

And also for realizing $A+B$, $\overline{A}+B$, $A+\overline{B}$ and $\overline{A}+\overline{B}$, both circuit block (7) and (8) are activated using the voltage of control gate as shown in Table 2.

For realizing XOR and XNOR both circuit block (7) and (8) are activated.

For realizing A or $\overline{A}$, both (7) and (8) are activated. And also logic of $B+\overline{B}=1$ is used for the signal of B or $\overline{B}$.

For realizing 0, both circuit block (1) and (2) are set to off-state by using C1=C2=C5=C6=-V.

For realizing 1, both circuit block (1) and (2) are set to on-state by using C1=C2=C3=C4=C5=C6=C7=C8=0. Therefore, 1 is realized by using $A+\overline{A}=1$ and $B+\overline{B}=1$.

Using the circuit shown in Fig.5 16 functions can be realized with 14 DG-MOSFET. This value of 14 is larger than that 12 for (+V, 0) case. Therefore, for realizing 16 functions (+V, 0) scheme is suitable for realizing small number of DG-MOSFET compared to that with (-V, 0) scheme.

3 Derivation of 12T DRDLC using three states (+V, 0, -V) from newly proposed two states scheme

In section 2 for realizing 16-functions with 2 states of control gate voltages 12T DRDLC using (+V, 0) scheme and 14T DRDLC using (-V,0) scheme have been newly proposed. If three states (+V, 0, -V) of control gate voltages can be realized, the number of DG-MOSFETs will be reduced from 12-14 of 2 states scheme.

Contrary to 12T DRDLC using (+V, 0) case, the off-state can be realized with only one DG-MOSFET for (+V, 0, -V) case. Therefore, logic of $A\cdot\overline{A}=0$ required for (+V, 0) case is not needed for (+V, 0, -V) case. This fact leads to the expectation for removing two DG-MOSFET controlled by C2 and C5. However, if these DG-MOSFETs are removed from Fig.3, four logics $\overline{A}B$, $\overline{A}\overline{B}$, $\overline{A}+B$ and $\overline{A}+\overline{B}$, can not be generated. Therefore, number of DG-MOSFET can not be reduced less than 12, even if three states (+V, 0, -V) of control gates voltages is introduced.

For 14T DRDLC using (0, -V) case, the on-state can be realized with only one DG-MOSFET for (+V, 0, -V) case. Therefore, logic of $B+\overline{B}=1$ required for (0, -V) case is not needed for (+V, 0, -V) case. This fact leads to the expectation for

removing two DG-MOSFET controlled by C4 and C7 from Fig.5. Fortunately, if these DG-MOSFETs are removed, 16 functions can be successfully realized. This is because, these two DG-MOSFETs are used only for realizing on-state for (0, -V) case.

As a result, by introducing three states (+V, 0, -V), 14T DRDLC with two states (0, -V) can be improved to 12T DRDLC with three states (+V, 0, -V) as shown in Fig.7. Configuration inputs and corresponding logic functions of Fig.7 is shown in Table 3.

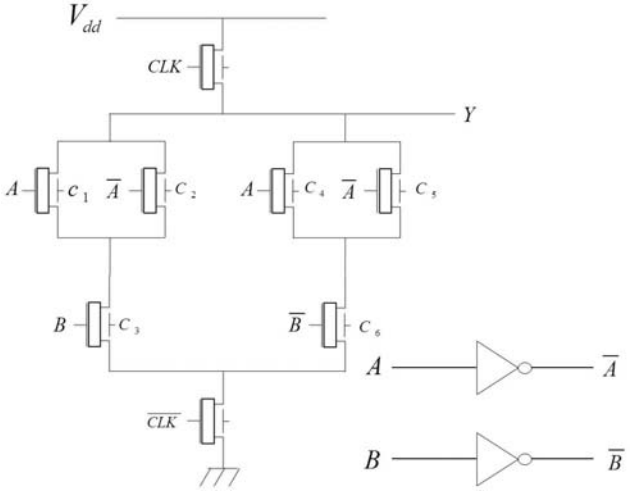


Figure 7: Newly proposed 16-function 12T DRDLC with three states (+V, 0, -V).

Table 3: Configuration inputs and corresponding logic functions for newly proposed 16-function 12T DRDLC with three states (+V, 0, -V).

C_1	C_2	C_3	C_4	C_5	C_6	$\overline{Y}$
0	-V	0	+V	+V	+V	AB
-V	0	0	+V	+V	+V	$\overline{A}B$
+V	+V	+V	0	-V	0	$A\overline{B}$
+V	+V	+V	-V	0	0	$\overline{A+B}$
-V	0	0	0	-V	0	$A \oplus B$
0	-V	0	-V	0	0	$\overline{A \oplus B}$
0	-V	+V	0	-V	+V	A
-V	0	+V	-V	0	+V	$\overline{A}$
+V	-V	0	+V	-V	+V	B
+V	-V	+V	+V	-V	0	$\overline{B}$
+V	-V	0	0	-V	+V	$A+B$
+V	-V	0	-V	0	+V	$\overline{A}+B$
0	-V	+V	+V	-V	0	$A+\overline{B}$
-V	0	+V	-V	+V	0	$\overline{A}+\overline{B}$
0	0	+V	0	0	+V	T
-V	-V	0	0	0	0	$\perp$

As a result, even if three states (+V, 0, -V) scheme is introduced, the minimum number of DG-MOSFET is 12 as the same as two states (+V, 0) case as shown in Table 4. For three states case different structure of circuits of Fig.3 and Fig.7 can be realized using 12 DG-MOSFETs.

Table 4: Reduction of number of DG-MOSFETs with increasing states for control gate voltages.

	Two states	Three states
Number of DG-MOSFETs	**12 (+V, 0)** ⇨	**12 (+V, 0, -V)**
	14 (0, -V) ⇨	**12 (+V, 0, -V)**

4 Relationship between DG-MOSFET used in this paper and previously proposed Independent-gate controlled Double Gate transistor[6]-[9]

In the previous sections 16 functions 12-14T DRDLC with two states, (+V, 0) or (0, -V) and 12T DRDLC with three states (+V, 0, -V) case have been described. In this section relationship between proposed these DRDLC and Independent-gate controlled Double Gate transistor (IDG MOSFET) reported in ref[6]-[9] is described.

The configuration of OR type IDG MOSFET is shown in Fig.8 (A). A and B are input signals. Obtained configuration is OR, A+B, as shown in this figure. This type of DG MOSFET can be realized with optimized impurity concentration of body of MOSFET such as FinFET. By using this IDG MOSFET two conventional FinFETs connected in parallel can be replaced by one IDG MOSFET. This OR type IDG MOSFET is promising candidate for replacing presently available FinFET. The configuration of AND type IDG MOSFET is shown in Fig.8 (B). A and B are input signals. Obtained configuration is AND, AB, as shown in this figure. This type of DG MOSFET can be realized with optimized impurity concentration which is different value compared to that of OR case and optimized gate oxide thickness. By using this IDG MOSFET two conventional FinFETs connected in series can be replaced by one IDG MOSFET. OR type IDG MOSFET is easy to fabricate compared to AND type because of easiness of optimization of device parameters.

A	B	State of FET
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

(A)

A	B	State of FET
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

(B)

Figure 8: Configuration of IDG-MOSFET, (A) OR type IDG-MOSFET, (B) AND type IDG-MOSFET.

(A)

A	B	State of FET
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

(B)

A	Cont	State of FET
0	0	OFF
0	+V	ON
1	0	ON
1	+V	ON

If +V=1, the same configuration.

Figure 9: Configuration of OR type IDG MOSFET(A) and DG-MOSFET with two states (+V, 0) (B).

The configuration of newly proposed DG-MOSFET with two states (+V, 0) case is shown in Fig.9 with OR type IDG MOSFET of Fig.8 (A). It is clear that the configuration of DG-MOSFET with two states (+V, 0) case is the same as that of OR type IDG MOSFET, if +V is equal to the amplitude of input signals, A and B. This leads to the fact that newly proposed DG-MOSFET with two states (+V, 0) case can be successfully realized by using presently available OR type IDG MOSFET.

(A)

A	B	State of FET
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

(B)

A	Cont	State of FET
0	-V	OFF
0	0	OFF
1	-V	OFF
1	0	ON

If -V→ 0 and 0→1 for Cont, (B) is the same configuration as (A).

Figure 10: Configuration of AND type IDG MOSFET(A) and DG-MOSFET with two states (0, -V) (B).

The configuration of newly proposed DG-MOSFET with two states (0, -V) case is shown in Fig.10 with AND type IDG MOSFET of Fig.8 (B). It is clear that the configuration of DG-MOSFET with two states (0, -V) case is the same as that of AND type IDG MOSFET, if configuration of input of –V, 0 for (0, -V) case are changed to 0, 1 as shown in Fig.10. This leads to the fact that newly proposed DG-MOSFET with two states (0, -V) case can be successfully realized by using AND type IDG MOSFET by changing control signals of –V and 0.

	A	Cont	State of FET
(5)	0	-V	OFF
(1)	0	0	OFF
(6)	1	-V	OFF
(2)	0	0	ON
(3)	1	+V	ON
(4)	1	+V	ON

Figure 11: Configuration of DG-MOSFET with three states (+V, 0, -V).

The configuration of DG-MOSFET with three states (+V, 0, -V) case is shown in Fig.11. The configuration (1)-(4) are the same as that of OR type IDG MOSFET case. The configuration of (5) can be easily realized if (1) can be realized. This is because due to the back gate effect[13] the threshold voltage of (5) is larger than (1) case for NMOSFET. On the other hand, the configuration of (6) can not be realized without further development of DG-MOSFET. This is because for realizing both (2) and (6) configuration further optimization of impurity concentration which is different from OR and AND type case is required.
These discussions are summarized in Fig.12. For realizing future DRDLC small number of DG-MOSFET and the consistency to the presently available IDG-MOSFET are key issues. From these point of view, 12T DRDLC with two sates (+V, 0) case are promising candidate for realizing future reconfigurable LSI.

Number of DG-MOSFETs	States of control gate
12	(+V, 0) = OR type IDG-MOSFET
14	(-V, 0) ⇨ (0, 1) = AND type IDG-MOSFET
12	(+V, 0, -V) ⇦ OR type IDG-MOSFET

Further development of device parameter is required.

Figure 12: Summary of this section. Status of DG-MOSFET.

4 Conclusion

Circuit design of 2-input reconfigurable dynamic logic based on double gate MOSFETs with the whole set of 16 functions has been newly described. 16 function 12T DRDLC with two states (+V, 0) of control gate voltages and 14T DRDLC with two states (0, -V) of control gate voltages have been newly proposed. From these two states control gate case, 12T DRDLC with three states (+V, 0, -V) of control gate voltages is successfully derived. Newly proposed DG-MOSFET with two states (+V, 0), (0, -V) cases can be successfully realized using presently available OR type, AND type IDG-MOSFET, respectively. Newly proposed circuit design, especially for 16 functions 12T DRDLC with two states (+V, 0) case is the promising candidates for realizing future reconfigurable LSIs.

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