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Proposal of Independent-gate Controlled Double Gate SGT and its Application to Logic Circuit

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Abstract

Independent-gate controlled Double Gate SGT (DG SGT) has been newly proposed. Three kinds of DG SGT which use rectangular parallelepiped, U-shaped, and doughnut-shaped silicon pillar have been described. The reduction of pattern area of logic circuit such as inverter and NAND circuit with DG SGT has been estimated. Using DG SGT the pattern area of NAND circuit of small channel width can be reduced to 53-65% compared to that of conventional SGT. Using DG SGT the pattern area of inverter and 4-input NAND with large channel width of 40F can be reduced to 70-75%. Furthermore, the fabrication cost of logic circuit with DG SGT has been described. DG SGT is the promising candidates for realizing small pattern area and low fabrication cost for logic circuit and LSI.

Keywords: Double Gate, SGT, FinFET, pattern area, LSI, logic circuit

1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem various kinds of 3D transistors has been proposed. FinFET [2][3] which use the 3 planes as the channel for reducing the short channel effect has been developed. The application of FinFET to high end MPU begins[4][5]. Another candidates for replacing the conventional planar transistor is SGT (Surrounding Gate Transistor) [6][7] . SGT uses the 4 planes as the channel. Therefore, with the scaling of SGT, small pattern area of LSI such as logic circuit can be realized compared to that of conventional planar transistor[8][9]. Furthermore because of its merit for easiness of stacking structure SGT is used not only to logic circuit but also memory devices[10][11][12].

On the other hand for reducing the pattern area and number of transistors for logic circuit Independent-gate controlled Double Gate transistor, DG transistor, has been proposed[13]. Independent-gate controlled Double Gate transistor uses the sidewall as the channel. This leads to the reduction of pattern area as the same as FinFET case. Independent-gate controlled Double Gate transistor uses two independent input. Therefore, two conventional planar transistors connected in series or parallel can be reduced to one Independent-gate controlled Double Gate transistor by controlling device parameters such as the impurity concentration of body or gate oxide thickness[14]. Furthermore, the pattern area reduction of logic circuit with Independent-gate controlled Double Gate transistor compared to that with the conventional planar transistor and FinFET has been reported[15][16][17]. Independent-gate controlled Double Gate type SGT (DG SGT) which will be useful for reducing the pattern area and the number of the transistors has not been reported. In this paper DG SGT and its application to logic circuit have been newly proposed.

This paper is organized as follows. Section 2 describes the structure and process technology of 3 kinds of DG SGTs (DG1 SGT, DG2 SGT, and DG3 SGT). Section 3 describes the pattern design of logic circuit such as inverter and NAND gate with newly proposed DG SGT. Section 4 presents the reduction of pattern area and fabrication cost of these logic with DG SGT. Finally, a conclusion of this work is provided in Section 5.

2 Structure and process technology of newly proposed DG SGT

Conventional SGT which use the 4 planes as the channel is shown in Fig.1. Four sidewalls can be used as the channel. Assuming that the sidewall channel width is defined as Ws, within the small pattern area large total channel width of 4Ws can be successfully realized. If Ws=2F, where F is design rule, 4Ws=8F as shown in Fig.1. The drain current flows along vertical direction which is perpendicular to

the conventional planar transistor case.

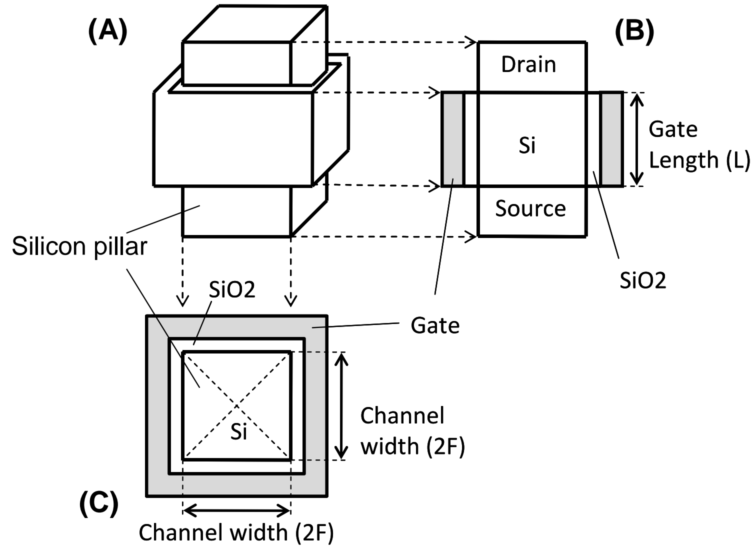


Figure 1: Conventional SGT with silicon pillar size of 2F*2F. (A)Structure, (B)Cross-sectional view, (C)Top view.

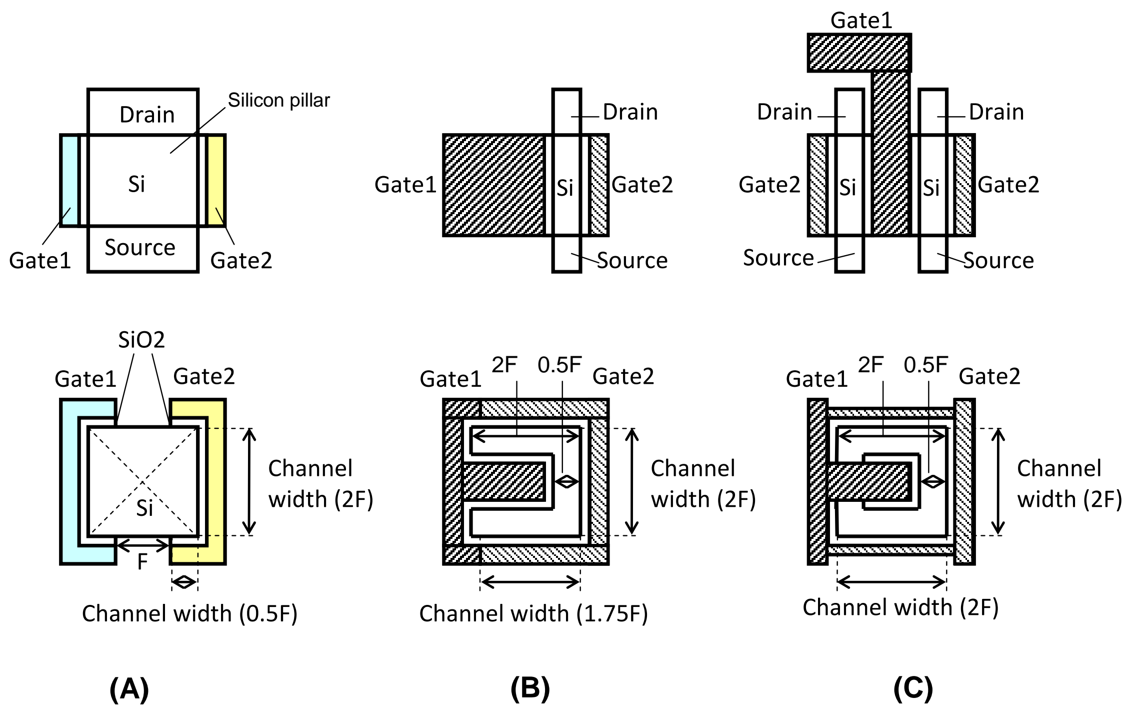


Figure 2: Newly proposed 3 kinds of DG SGT. Upper figure shows the cross-sectional view and lower figure shows the top view. (A)DG1 SGT, (B)DG2 SGT, (C)DG3 SGT.

Newly proposed 3 kinds of DGT are shown in Fig.2(A)-(C). Upper figure shows the cross-sectional view and lower figure shows the top view.
First DG SGT, DG1 SGT, is shown in Fig.2(A). Independent gates, Gate1 and Gate2 are fabricated at the same process step and mask. The minimum distance between Gate1 to Gate2 is minimum design rule of F. The silicon pillar of 2F*2F is controlled with Gate1 and Gate2 as the same as ref[13]-[16]. The channel width for Gate1 and Gate2 is the same value of 2F+0.5F*2=3F as shown in the top view.
Second DG SGT, DG2 SGT, is shown in Fig.2(B). The shape of silicon pillar is U-shaped. Width of silicon pillar is 0.5F. After the formation of Gate1, Gate2 is fabricated using the different mask. Therefore, Gate2 can be stacked on the Gate1 via the dielectrics formed between Gate1 and Gate2. As a result, the distance between Gate1 to Gate2 can be reduced to 0F. The channel width for Gate1 is 1.5F*2+F+0.5F*2+0.25F*2=5.5F. The channel width of Gate2 is the same value of 1.75F*2+2F=5.5F. This large and the same channel width of 5.5F compared to DG1 SGT is feature of DG2 SGT case.
Third DG SGT, DG3 SGT, is shown in Fig.2(C). The shape of silicon pillar is doughnut-shape. Width of silicon pillar is 0.5F. With the formation of sidewall gate, gates in the inner wall and the external wall of the silicon pillars are fabricated. After that Gate1 and Gate2 are fabricated sequentially using the different mask. The channel width for Gate1 which is formed in inner wall is 4F. The channel width for Gate2 which is formed in external wall is 8F. This different channel width of 4F and 8F and large total channel width of 4F+8F=12F, (11F for DG2 SGT, 6F for DG1 SGT case), are the feature of DG3 SGT case.

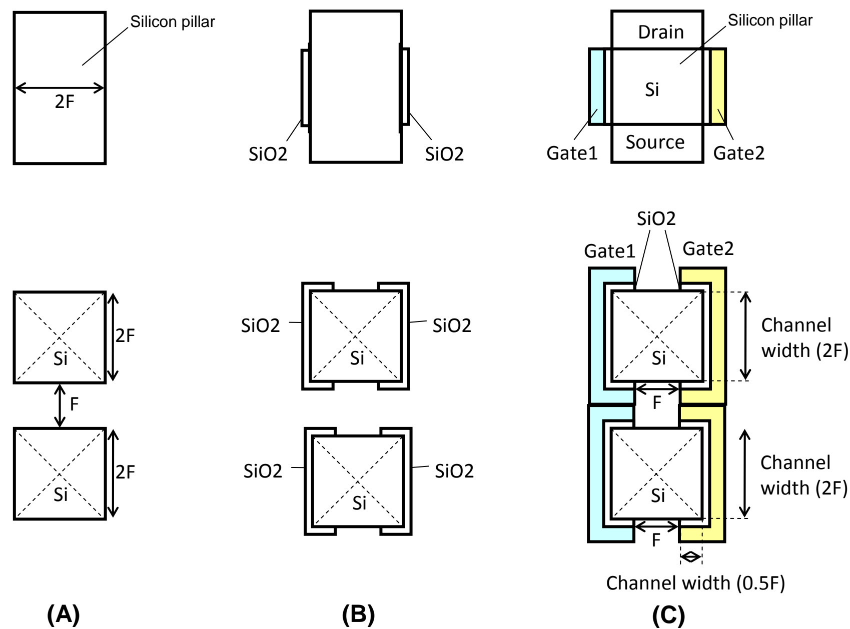


Figure 3: Process step of DG1 SGT. Upper figure shows cross-sectional view and lower figure shows top view. (A)Silicon pillar formation, (B)Formation of gate oxide, (C)Formation of gate electrode.

The process flow of newly proposed DG SGTs are shown in Fig.3-5. As shown in the top view two adjacent silicon pillars are described.
The process flow of DG1 SGT is shown in Fig.3. At first, the silicon pillar of 2F*2F is fabricated as shown in Fig.3(A). After the oxidation for gate, the oxide besides the channel region is removed using photo etching process as shown in Fig.3(B). Finally, Gate1 and Gate2 are fabricated at the same time with the same mask as shown in Fig.3(C).

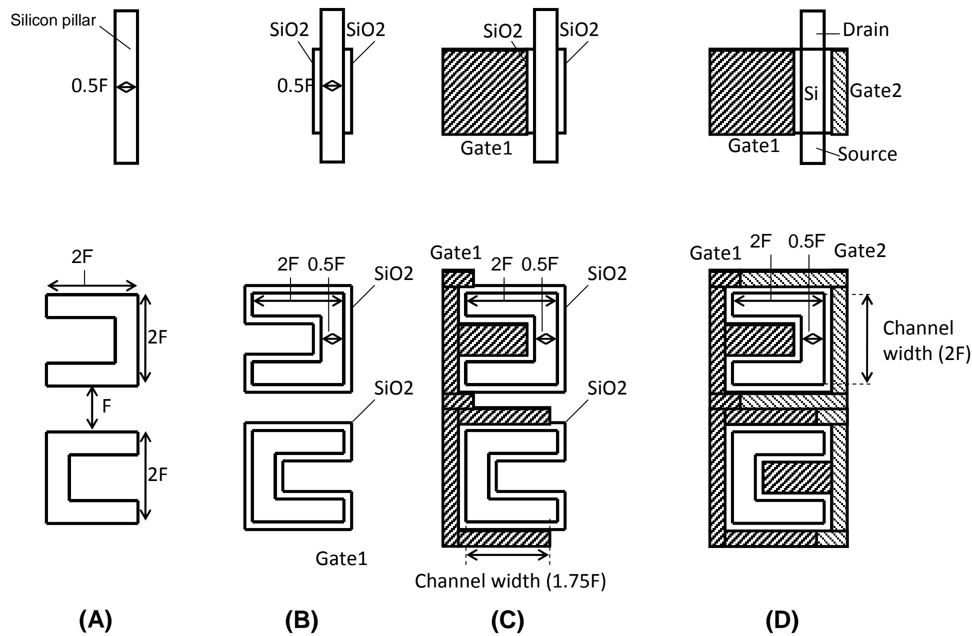


Figure 4: Process step of DG2 SGT. Upper figure shows cross-sectional view and lower figure shows top view. (A)Silicon pillar formation, (B)Formation of gate oxide, (C)Formation of Gate1, (D)Formation of Gate2.

The process flow of DG2 SGT is shown in Fig.4. After the formation of silicon pillar of 2F*2F, the silicon pillar of width of 0.5F is fabricated by etching the silicon pillar using photo mask process. The formation of silicon pillar of 2F*2F and etching of this silicon pillar are fabricated using different mask. The channel width difference between Gate1 and Gate2 caused by the miss-alignment of these two masks can be successfully cancelled using the U-shaped pattern layout of silicon pillar as shown in Fig.4(A). After that, the oxidation for gate oxide is formed as shown in Fig.4(B). Next Gate1 is formed using mask as shown in Fig.4(C). After the formation of dielectrics on the Gate1, Gate2 is formed using another mask as shown in Fig.4(D). Therefore, Gate1 and Gate2 can be electrically separated.
The process flow of DG3 SGT is shown in Fig.5. After the formation of silicon pillar of 2F*2F, the silicon pillar of doughnut-shape is fabricated by using phase shift mask[18]. The pillar width of doughnut-shape is 0.5F. After that, the oxidation for gate oxide is formed as shown in Fig.5(A).

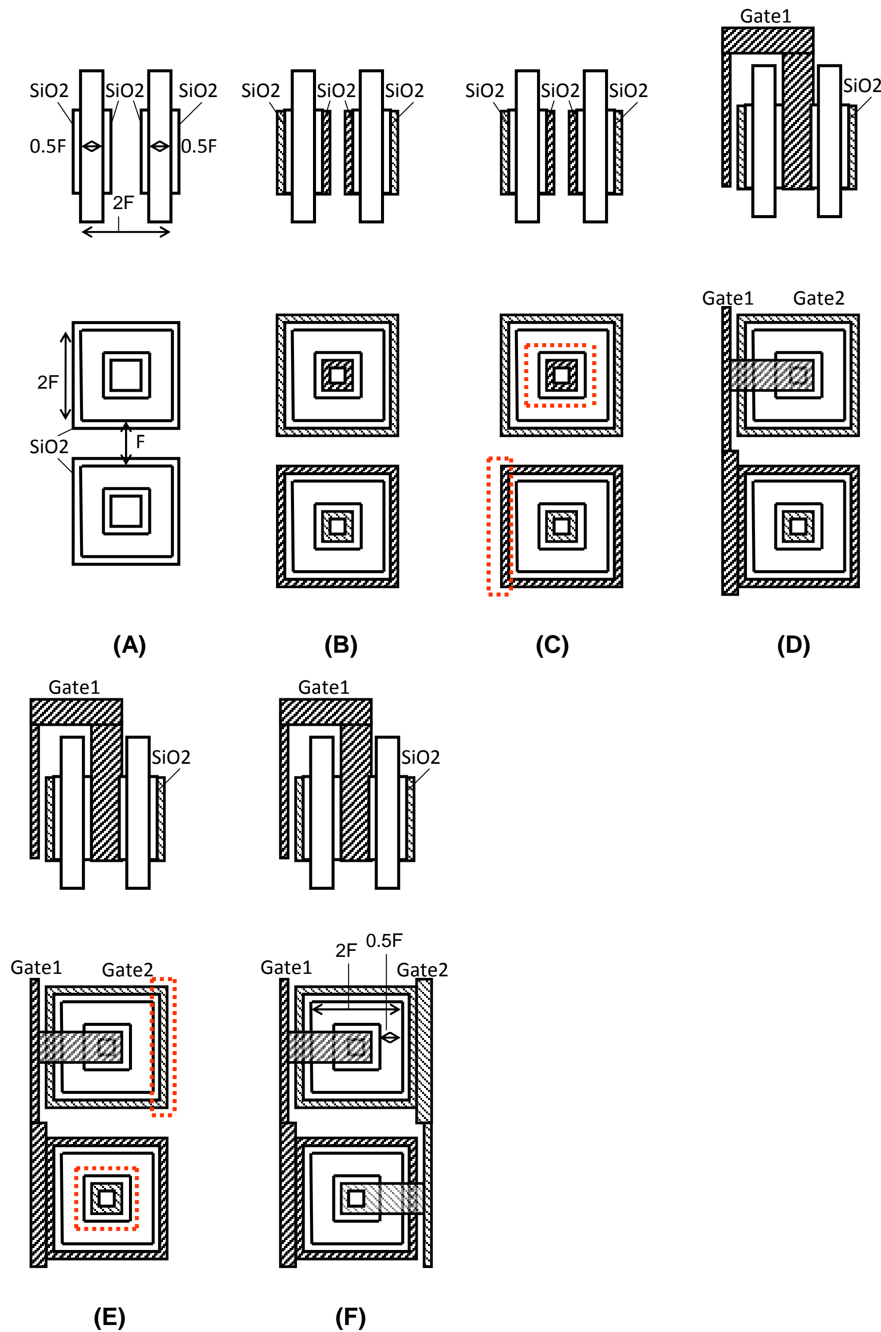


Figure 5: Process step of DG3 SGT. Upper figure shows cross-sectional view and lower figure shows top view. (A)Formation of gate oxide, (B)Formation of sidewall gate, (C)Etching of dielectric for Gate1, (D)Formation of Gate1, (E) Etching of dielectric for Gate2, (F)Formation of Gate2.

Then the sidewall gates are formed to the inner wall and the external wall of the doughnut-shaped silicon pillar by using etch-back process as shown in Fig.5(B). After the formation of dielectric on the gate electrode, this dielectric within the

dotted line is removed for connecting Gate1 as shown in Fig.5(C). Then Gate1 is formed using mask, (Fig.5(D)). After the formation of dielectric on the gate electrode, this dielectric within the dotted line is removed for connecting Gate2 as shown in Fig.5(E). Then Gate2 is formed using mask, (Fig.5(F)). Using these process steps the channel width of DG3 SGT becomes equal value of 8F+4F=12F, if even DG3 SGTs are connected in parallel.

3 Pattern design of logic circuit using proposed DG SGT

In this section pattern design of logic circuit such as inverter and NAND gate using newly proposed 3 kinds of DG SGT is described. Design rule for pattern design is shown in Table 1.

Table 1: Design rule for pattern layout.

	Conv.SGT	DG1 SGT	DG2,3 SGT
Gate length	F	F	F
Wiring	F	F	F
Wiring to Wiring (same)	F	F	F
Wiring to Wiring (diff.)	0.5F	0.5F	0.5F
Well isolation	3F	3F	3F
Contact size	F×F	F×F	F×F
Silicon pillar size	2F×2F	2F×2F	2F×2F
Silicon pillar width	2F	2F	0.5F
Gate1 to Gate2	——	F	0F
AA to silicon pillar	0.5F	0.5F	0.5F
Gate to contact	0.5F	0.5F	0.5F
Gate to direct contact	—	—	0F
Direct contact size	—	—	F×F

Except for the Gate1 to Gate2, design rule of DG1 SGT is the same as that of conventional SGT. Gate to contact on the silicon pillar is as large as 0.5F. This relatively relaxed design rule enables to use the conventional photo mask process. As a result, the pillar size becomes as large as 2F*2F. Compared DG1 SGT to DG2,3 SGT, silicon pillar width of 0.5F and Gate1 to Gate2 of 0F should be noticeable. This small pillar size of 0.5F can be realized using relatively large pillar size of 2F*2F. Small pillar size enables to suppress the short channel effect of DG SGT. Distance of Gate1 to Gate2 of 0F enable to realize the larger channel width of DG2,3 SGT compared to that of DG1 SGT and conventional SGT as shown in the next section. Furthermore, direct contact between drain electrode to

wiring is newly introduced for DG2,3 SGT case. This direct contact is indispensable for the connection between drain electrode with the small width of 0.5F to large contact area of F*F. For the pattern design of logic circuit β ratio of 2 is adopted[19].

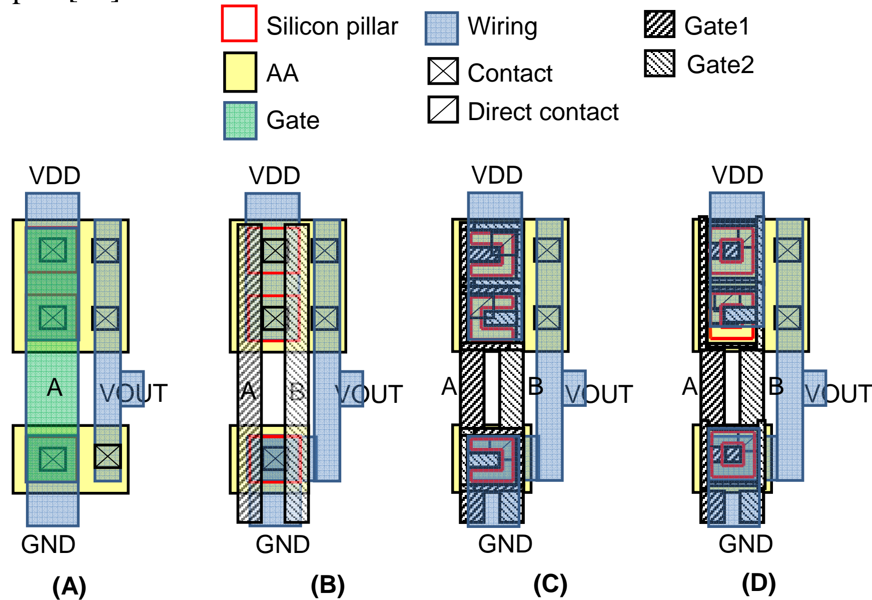


Figure 6: Pattern of inverter with SGT using pillar size of 2F*2F. Pattern area is $5.5F*13F=71.5F^2$. (A)Conventional SGT, (B)DG1 SGT, (C)DG2 SGT, (D)DG3 SGT.

The pattern of inverter with the minimum channel width is shown in Fig.6. The pattern of inverter is consisted to one pillar for NMOS and two pillars for PMOS. The pattern area of $5.5F*13F=71.5F^2$ for DG SGT is the same as that of conventional SGT. The obtained minimum channel width for NMOS are 8F for conventional SGT, 3F for DG1 SGT, 5.5F for DG2 SGT, and 4F/8F for DG3 SGT. The obtained minimum channel width for DG SGT is smaller than that of conventional SGT. This minimum channel width can be realized by connecting Gate2 to Vss. Furthermore, maximum channel width using pattern of Fig.6 is realized by connecting Gate1 to Gate2 for DG SGT. The values are as large as 6F for DG1 SGT, 11F for DG2 SGT, and 12F for DG3 SGT. The obtained maximum channel width of DG2 and DG3 SGT are larger than that of conventional SGT. Therefore, by using this inverter pattern both smaller and larger cannel with of DG2,3 SGT can be successfully realized compared with that of conventional SGT. The pattern of 2-input NAND circuit with the minimum channel width is shown in Fig.7. The pattern area $5.5F*13F=71.5F^2$ of DG SGT is smaller than that of conventional SGT of $8.5F*13F=110.5F^2$. This value is 64.7% of that of conventional SGT. This small pattern area of DG SGT is caused by the reduction of number of transistors which is the merit of Independently controlled DG transistor. Minimum channel width for 2-input NAND circuit is the same as that of inverter. For NAND circuit case the maximum channel width as the inverter case can not be realized. This is because all input signal to gate is used as the independent input signal.

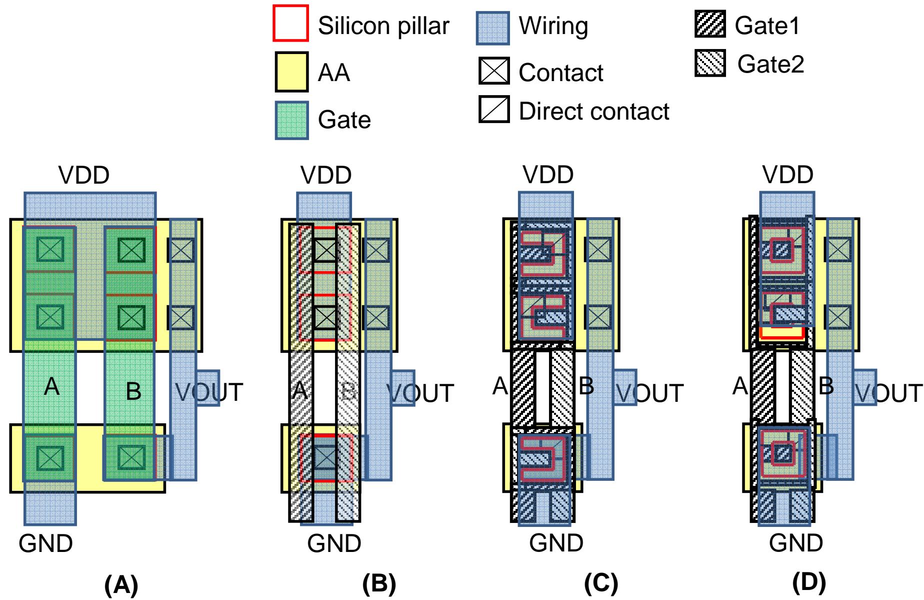


Figure 7: Pattern of 2-input NAND circuit with SGT using pillar size of 2F*2F. Pattern area is 5.5F*13F=71.5F^2 for DG SGT and 8.5F*13F=110.5F^2 for conventional SGT. (A)Conventional SGT, (B)DG1 SGT, (C)DG2 SGT, (D)DG3 SGT.

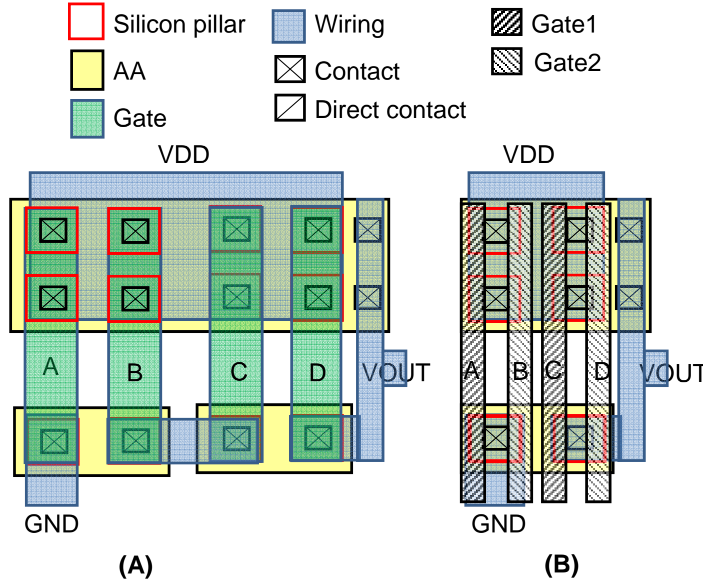
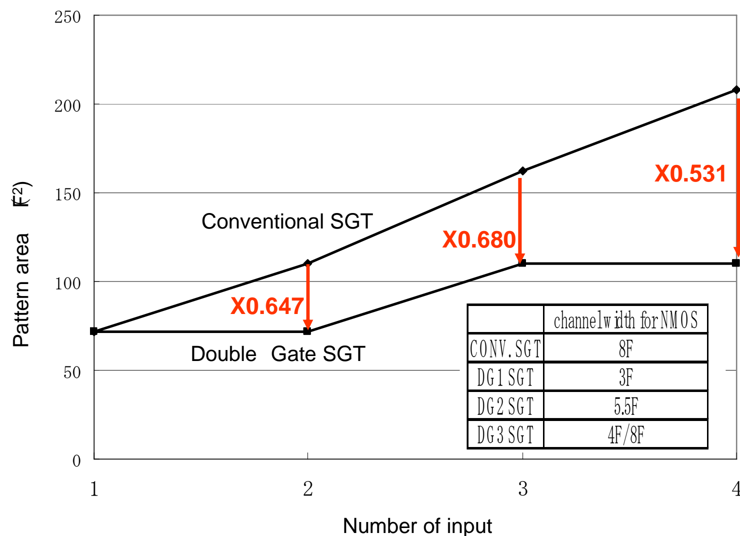


Figure 8: Pattern of 4-input NAND circuit with SGT using pillar size of 2F*2F. Pattern area is 8.5F*13F=110.5F^2 for DG SGT and 16F*13F=208F^2 for conventional SGT. (A)Conventional SGT, (B)DG1 SGT.

The pattern of 4-input NAND circuit with the minimum channel width is shown in Fig.8. The pattern area 8.5F*13F=110.5F^2 of DG1 SGT is the smaller than that of conventional SGT of 16F*13F=208F^2. This value is 53.1% of that of conventional SGT. This reduction rate is larger than that of 2-input NAND circuit case. The pattern area with DG2,3 SGT is the same as that of DG1 SGT.

4 Reduction of pattern area and fabrication cost of logic circuit with proposed DG SGT

In the previous section pattern design of logic circuit using proposed DG SGT has been described. In this section by using these results reduction of pattern area and fabrication cost of logic circuit with proposed DG SGT compared to that with conventional SGT has been estimated.



	channel width for NMOS
CONV.SGT	8F
DG1 SGT	3F
DG2 SGT	5.5F
DG3 SGT	4F/8F

Figure 9: Pattern area reduction with DG SGT compared to that with conventional SGT for minimum channel width case.

Firstly reduction of pattern area of logic circuit with the small channel width using DG SGT has been estimated. For the system LSI for communication the used channel width is relatively small. In the case of ref[20] 73.9% of transistor used channel width of 5F. In the conventional SGT case the minimum channel width is as large as 8F. For realizing the small effective channel width series connection of conventional SGT or large gate length must be introduced. Introduction of these technology suffer from large increase of pattern area and process cost. On the other hand the minimum channel width of the newly proposed DG SGT are 3F for DG1 SGT, 5.5F for DG2 SGT, and 4F/(8F) for DG3 SGT. These values are suitable for LSI for communication such as ref[20]. Furthermore, these small channel widths can be successfully realized with smaller pattern area compared to that with conventional SGT. The estimated value is shown in Fig.9. For NAND circuit case the pattern area using DG SGT with the minimum channel width can be reduced to 0.531-0.647 compared to that of conventional SGT. The reduction rate are the same value between 3 kinds of DG SGTs. These results shows that logic circuit with DG SGT is promising candidate for realizing small pattern size logic circuit with small channel width.

Next the reduction of pattern area of logic circuit with the large channel width using DG SGT has been estimated. For the system LSI such as embedded memory there are some buffer circuit with the relative large channel width. In the case of ref[21][22] 90% of transistor used channel width more than 20F. Even ref[20] which features short channel width employs 15.1% of transistor more than 20F. Therefore, pattern area of logic circuit with DG SGT and conventional SGT vs the channel width from minimum channel width to 40F have been estimated. The pattern area of inverter is shown in Fig.10. Except DG1 SGT, DG SGT realizes the smaller pattern area compared with conventional SGT case. This is because DG2,3 SGT can realize larger channel width compared to conventional SGT using the same pattern area. In the W=40F case, the pattern area is reduced to 0.752 for DG2 SGT and 0.697 for DG3 SGT compared to conventional SGT case.

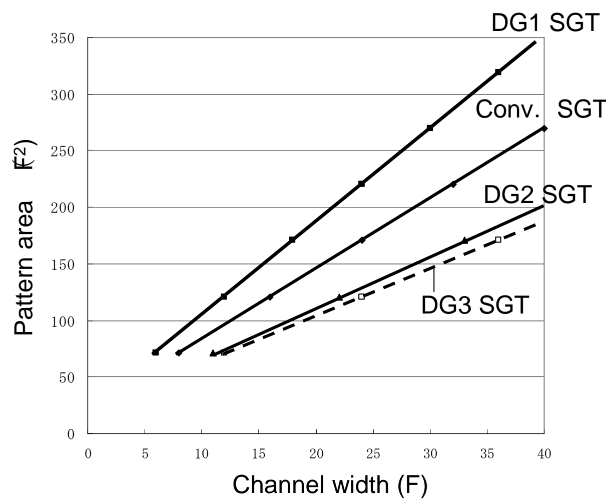


Figure 10: Pattern area comparison of inverter circuit between DG SGT and conventional SGT. Estimated channel width is from minimum channel width to 40F.

The pattern area of 2-input NAND circuit is shown in Fig.11. Except DG1 SGT, DG SGT realizes the smaller pattern area compared with conventional SGT case. However, the reduction rate is smaller compared with inverter circuit case. This is because used channel width for one input is small compared with conventional SGT case. However, the effect of reduction of transistor number with DG SGT enables to realize the smaller pattern area compared with conventional SGT case. In the W=40F case, the pattern area is reduced to 0.911 for DG2 SGT and 0.860 for DG3 SGT compared to conventional SGT case.

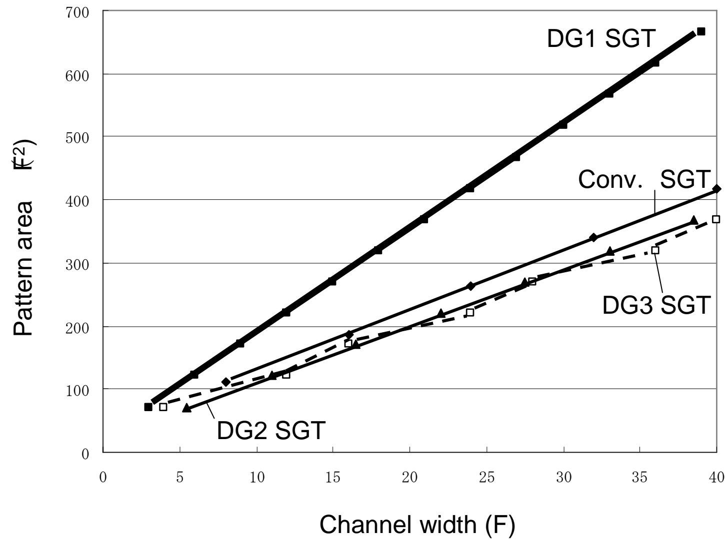


Figure 11: Pattern area comparison of 2-input NAND circuit between DG SGT and conventional SGT.

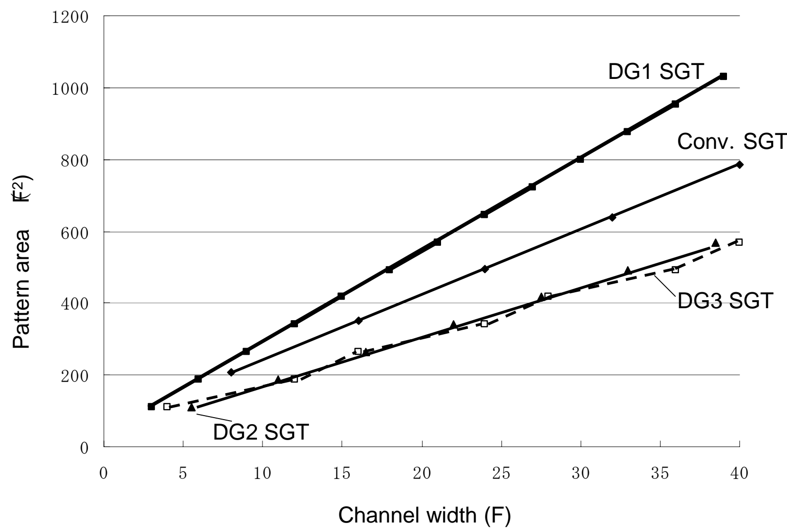


Figure 12: Pattern area comparison of 4-input NAND circuit between DG SGT and conventional SGT.

The pattern area of 4-input NAD circuit is shown in Fig.12. Except DG1 SGT, DG SGT realizes the smaller pattern area compared with conventional SGT case. The reduction rate is almost the same as inverter circuit case. This is because small channel width used for one input is overcomed by the effect of reduction of transistor number with DG SGT. In the W=40F case, the pattern area is reduced to 0.749 for DG2 SGT and 0.706 for DG3 SGT compared to conventional SGT case.
Finally, reduction of fabrication cost of logic circuit with proposed DG SGT compared to that with conventional SGT has been estimated. For realizing DG SGT extra process steps and masks are introduced to those of conventional SGT.

In the DG1 SGT case gate oxide etching process has been added. In the DG2 SGT case formation of U-shaped pillar with additional mask and formation of Gate2 with additional mask have been added. In the DG3 SGT case in addition two masks used in DG2 SGT 2 extra masks for etching the dielectrics for Gate1 and Gate2 (Fig.5) are added. It is well known that by adding one mask about 1-3% of extra process steps are required[23]. Therefore it is assumed that process steps are increased by 1% (corresponding to 0.5 mask) for DG SGT1 case, 4% (corresponding to 2 masks) for DG2 and 8% (corresponding to 4 masks) for DG3 compared to conventional SGT case. It is well known that fabrication cost of 1 chip of LSI are in proportional to the pattern area and total number of process steps[24][25]. Therefore, for estimating the fabrication cost not only pattern area and but also total number of process steps must be taken into account. The fabrication cost of logic circuit using conventional and DG SGT is shown in Fig.13.

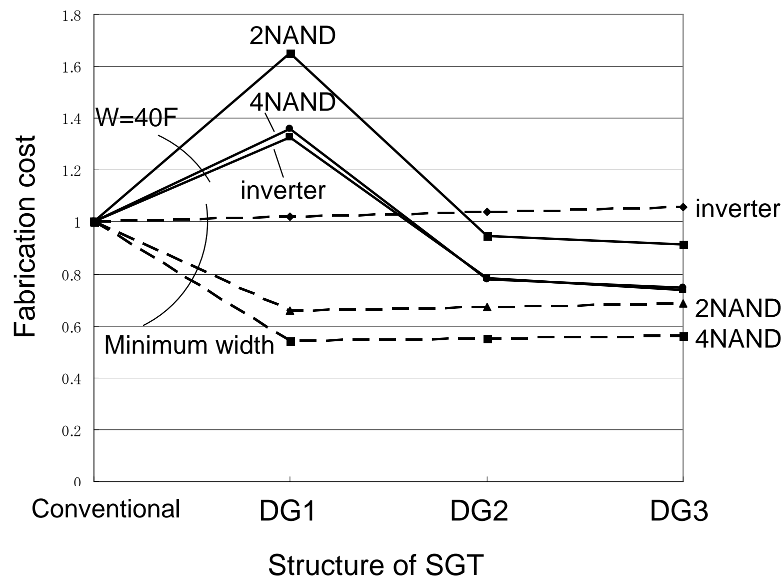


Figure 13: Fabrication cost of logic circuit using conventional and DG SGT.

The fabrication cost with conventional SGT is normalized as 1. For the minimum channel width case except inverter circuit the fabrication cost with DG SGT is smaller than conventional SGT case. For inverter case increase of process steps with DG SGT causes the increase of fabrication cost. For the channel width of 40F case except DG1 SGT, the fabrication cost for all kinds of logic circuit with DG2,3 SGT is smaller than that with conventional SGT case. This is because the effect of pattern area reduction described in the previous section successfully overcome the effect of number of process steps increase described in this section.

DG1 SGT which is useful for small channel width can be easily realized using DG2,3 SGT. Therefore, DG2,3 are promising candidates for reducing not only pattern area but also the fabrication cost of future logic circuit and LSI.

5 Conclusion

Independent-gate controlled Double Gate SGT (DG SGT) has been newly proposed. Three kinds of DG SGT which use rectangular parallelepiped, U-shaped, and doughnut-shaped silicon pillar have been described. The reduction of pattern area of logic circuit such as inverter and NAND circuit with DG SGT has been estimated. Using DG SGT the pattern area of NAND circuit of small channel width can be reduced to 53-65% compared to that of conventional SGT. Using DG SGT the pattern area of inverter and 4-input NAND with large channel width of 40F can be reduced to 70-75%. Furthermore, the fabrication cost of logic circuit with DG SGT has been described. DG SGT is the promising candidates for realizing small pattern area and low fabrication cost for logic circuit and LSI.

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