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Proposal of DTMOS Type SGT and its Application to Logic Circuit

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Abstract

The reduction of pattern area and delay time for logic circuit using newly proposed DTMOS type SGT with the same power consumption compared to that using conventional SGT are described. The reduction of delay time of logic circuit such as inverter and NAND circuit with small channel width using DTMOS type SGT is presented. The delay times of these circuits with DTMOS type SGT can be reduced to 64%-77% compared to that with conventional SGT with supply voltage of 0.5V. Furthermore, using large channel width transistor delay time or channel width with DTMOS type SGT can be reduced to 58%-61% compared to that with conventional SGT using supply voltage of 0.5V. DTMOS type SGT is the promising candidates for realizing high density high speed low power LSI.

Keywords: DTMOS, SGT, FinFET, pattern area, LSI, logic circuit

1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem various kinds of 3D transistors has been proposed. FinFET [2][3] which use the 3 planes as the channel for reducing the short channel effect has been developed. The application of FinFET to high end MPU begins[4][5]. Another candidates for replacing the conventional planar transistor is SGT (Surrounding Gate Transistor) [6][7] . SGT uses the 4 planes as the channel. Therefore, with the scaling of SGT, small pattern area of LSI such as logic circuit can be realized compared to that of conventional planar transistor[8][9]. Furthermore because of its merit for easiness of stacking structure SGT is used not only to logic circuit but also memory devices[10][11][12].
On the other hand for realizing high speed and low power operation planar type DTMOS (Dynamic Threshold MOS) has been proposed[13]. By connecting gate to substrate the threshold voltage of MOSFET can be dynamically controlled. Although maximum applied voltage is limited to 0.7V of forward bias for PN junction, this structure becomes increasingly important with reduction of supply voltage of LSI. Therefore, DTMOS type FinFET, application of DTMOS to FinFET, has been proposed[14][15]. For DTMOS type FinFET high speed and low power can be realized without increasing the pattern area. DTMOS type SGT which will be useful for low power and high speed operation as the same as FinFET case has not been reported. In this paper DTMOS type SGT and its application to logic circuit have been newly proposed. In this paper reduction of pattern area and delay time for logic circuit using newly proposed DTMOS type SGT with the same power consumption compared to that using conventional SGT are described.
This paper is organized as follows. Section 2 describes the structure, process technology, and performance of newly proposed DTMOS type SGT. Section 3 describes the reduction of pattern area and delay time of logic circuit using newly proposed DTMOS type SGT with the same power consumption compared to that using conventional SGT. Section 4 presents the pattern area and delay time comparison of transistor with large channel width between newly proposed DTMOS type SGT and conventional SGT. Finally, a conclusion of this work is provided in Section 5.

2 Structure, process technology, and performance of newly proposed DTMOS type SGT

Conventional SGT which use the 4 planes as the channel is shown in Fig.1. Four sidewalls can be used as the channel. Assuming that the sidewall channel width is

defined as Ws, within the small pattern area large total channel width of 4Ws can be successfully realized. If Ws=2F, where F is design rule, 4Ws=8F as shown in Fig.1. The drain current flows along vertical direction which is perpendicular to the conventional planar transistor case.

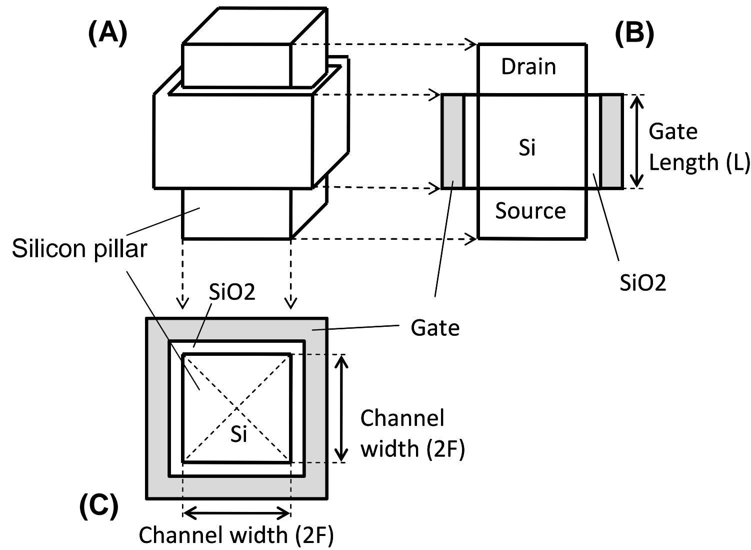

Figure 1: Conventional SGT with silicon pillar size of 2F*2F. (A)Structure, (B)Cross-sectional view, (C)Top view.

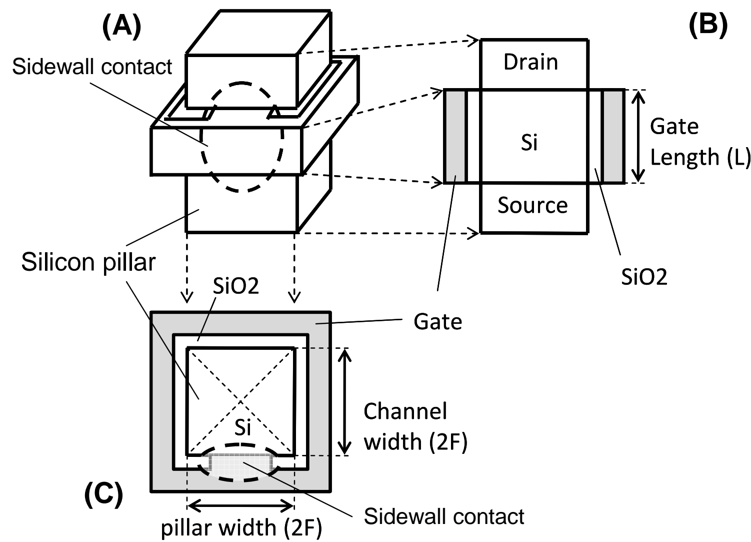

Figure 2: Newly proposed DTMOS type SGT with silicon pillar size of 2F*2F. (A)Structure, (B)Cross-sectional view, (C)Top view.

Newly proposed DTMOS type SGT is shown in Fig.2. The contact between gate and silicon pillar which corresponds to substrate is formed at the sidewall as shown in Fig.2 (A)(C). Therefore, extra pattern area for fabricating the sidewall

contact compared with that of conventional SGT is not required. Using this structure high speed operation and low power consumption compared to the conventional SGT can be realized. The maximum channel width of DTMOS type SGT is 4Ws-(width of sidewall contact). If Ws=2F and width of sidewall contact is F, 4Ws-(width of sidewall contact)=8F-F=7F as shown in Fig.2. This smaller channel width compared to that of conventional SGT with the same pillar side is important design issue for realizing logic circuit with DTMOS type SGT.

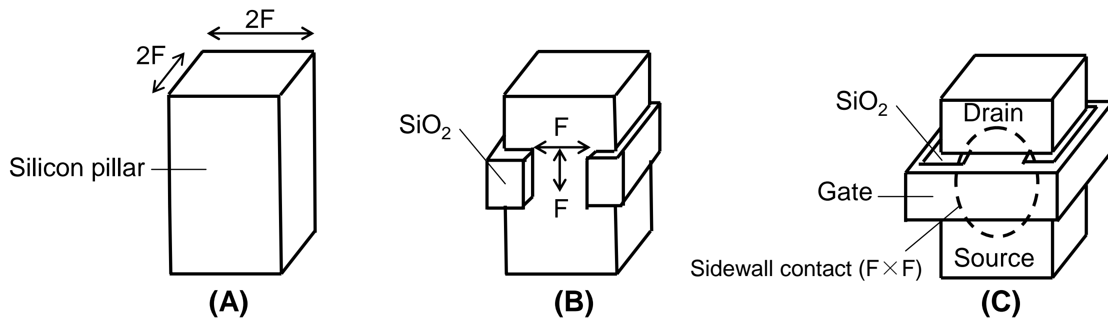

Figure 3: Process flow of DTMOS type SGT. (A)Formation of silicon pillar, (B)Formation of sidewall contact area, (C)Formation of sidewall contact and gate.

The formation of sidewall contact is very important issue for realizning DTMOS type SGT. The process flow of DTMOS type SGT is shown in Fig.3. At first, silicon pillar is fabricated as shown in Fig.3 (A). After the oxidation for gate oxide, the gate oxide of sidewall contact area is removed using photo etching process as shown in Fig.3 (B). Finally, sidewall contact and gate electrode is formed as shown in Fig.3 (C). Similar process technology is previously reported which realizes sidewall contact for stacked type FinFET in ref[15].
It is well known that LSI using DTMOS can realize higher speed and lower power consumption characteristics compared to LSI using conventional MOS using optimized threshold voltage. For example, if threshold voltage of on state, Vton=0.1V, threshold voltage of off state, Vtoff=0.3V for DTMOS and threshold voltage both on and off state, Vt=0.2V for conventional MOS is used, this characteristics can be realized for scaled MOSFET of 70nm. In this paper for calculating the reduction of pattern area and delay time with DTMOS type SGT under the same power conditions compared to conventional SGT, estimation is performed as follows.
For realizing the same power consumption between DTMOS type SGT and conventional SGT, Vtoff=Vt are fixed to the same value of 0.2V. The delay time of logic circuit, T_d, can be estimated using (1)[16].

$T_d=kC_LV_{DD}/(W(V_{DD}-Vton)^n)$ ----(1)

Where C_L, V_{DD}, W, k, n, and Vton are load capacitance of logic circuit, supply

voltage, channel width, constant of proportionality, constant of proportionality about mobility, and threshold voltage of on state, respectively. Vton can be estimated using (2).

$$Vton=Vtoff-\Delta Vt=Vt-\Delta Vt \text{ --------(2)}$$

Where ΔVt is substrate biasing effect of threshold voltage for DTMOS type SGT. When the delay time with conventional and DTMOS type SGT are the same value, (3) is obtained using (1)(2).

$$C_Lconv V_{DD}/(Wconv (V_{DD}-Vt)^n)= C_{LDTMOS} V_{DD}/(W_{DTMOS} (V_{DD}-Vt+\Delta Vt)^n) \text{ --(3)}$$

Where C_Lconv, C_{LDTMOS}, Wconv, and W_{DTMOS} are load capacitance with conventional SGT, load capacitance with DTMOS type SGT, channel width with conventional SGT, and channel width with DTMOS type SGT, respectively. From (3), (4) can be obtained.

$$1/m= W_{DTMOS}/Wconv=(C_{LDTMOS}/C_Lconv)((V_{DD}-Vt)/(V_{DD}-Vt+\Delta Vt))^n\text{----(4)}$$

(4) shows that for the same delay time condition channel width of DTMOS type SGT can be reduced to 1/m (m>1) compared to that of conventional SGT. 1/m is defined as channel width reduction rate. For the scaled MOSFET $(C_{LDTMOS}/C_Lconv)=1.1$, $\Delta Vt=0.2V$, and n=1.3 (n=2 for long channel MOSFET). Channel width reduction rate with DTMOS type SGT, 1/m, vs supply voltage using (4) is shown in Fig.4.

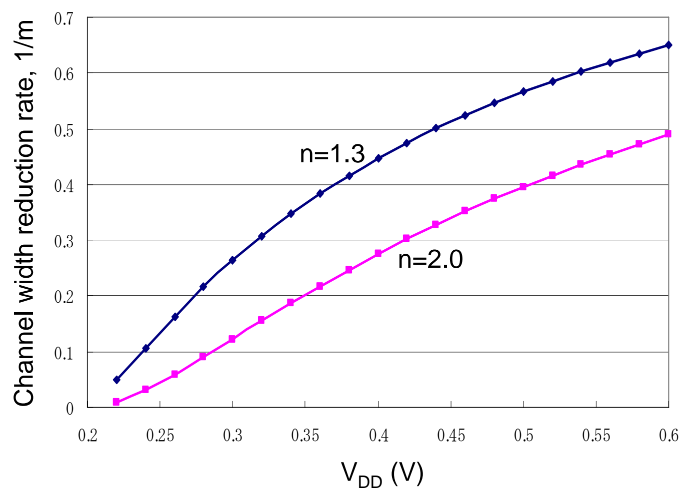

Figure 4: Channel width reduction rate, 1/m, using DTMOS type SGT vs supply voltage.

DTMOS type SGT is very effective for reducing the channel width or delay time for supply voltage range from 0.22V to 0.60V which is available to DTMOS structure. If 1/m is smaller than 1, smaller delay time or smaller pattern area compared to the conventional SGT case can be realized. For supply voltage of 0.5V and n=1.3 case, channel width reduction rate, 1/m, is as small as 0.57. In other words, For the DTMOS SGT case the same speed and power consumption characteristics can be realized with 0.57 times channel width compared to conventional SGT. This effect contributes to the reduction of pattern area or delay time.

For the SGT design the size of silicon pillar is very important. The design of DTMOS type SGT vs silicon pillar size is shown in Fig.5. The design of conventional SGT is also shown as a reference. The channel width of conventional SGT is shown with a solid line. The channel width is single value corresponding to pillar size. For example, the channel width is 8F, if pillar size is 2F*2F. On the other hand the channel width of DTMOS type SGT is not determined by only pillar size but by pillar size and sidewall contact width. This is because the channel width can be controlled by the sidewall contact width using (channel width)=4*(pillar size)-(sidewall contact width). For example, if pillar size is 2F*2F, the channel width F-7F can be successfully generated using sidewall contact width 7F-F. This is shown by the doted line in Fig.5 as physical channel width. Physical channel width is equal to geometrical channel width. Furthermore, in DTMOS case, under the same speed and power consumption condition the channel width can be reduced to 0.57 times to conventional SGT. In other words, the channel width of DTMOS is 1/0.57=1.77 times effective compared to conventional case. (channel width of conventional SGT)*1.77 is defined as effective channel width. In DTMOS type SGT case, if pillar size is 2F*2F, the channel width 1.77F-12.4F can be successfully generated using sidewall contact width 7F-F. This effective channel width is shown by the dashed line in Fig.5. Using the same pillar size both smaller and larger effective channel width compared to conventional SGT can be successfully realized for DTMOS type SGT. Conventional SGT has disadvantage of relatively large value of minimum channel width. Even if the smallest pillar size of F*F is used smaller channel width less than 4F can not be realized. This disadvantage limited the application of conventional SGT. However, for the DTMOS type SGT case the minimum effective channel width can be successfully reduced to 1.77F. This feature enables to realize wide application. Furthermore, with the same pillar size larger effective channel width can be realized compared to conventional SGT. For pillar size of 2F*2F case 12.4F/8F=1.55 times larger effective channel width can be realized. This feature leads to the reduction of transistor size and logic circuit with DTMOS type SGT as shown in the next section.

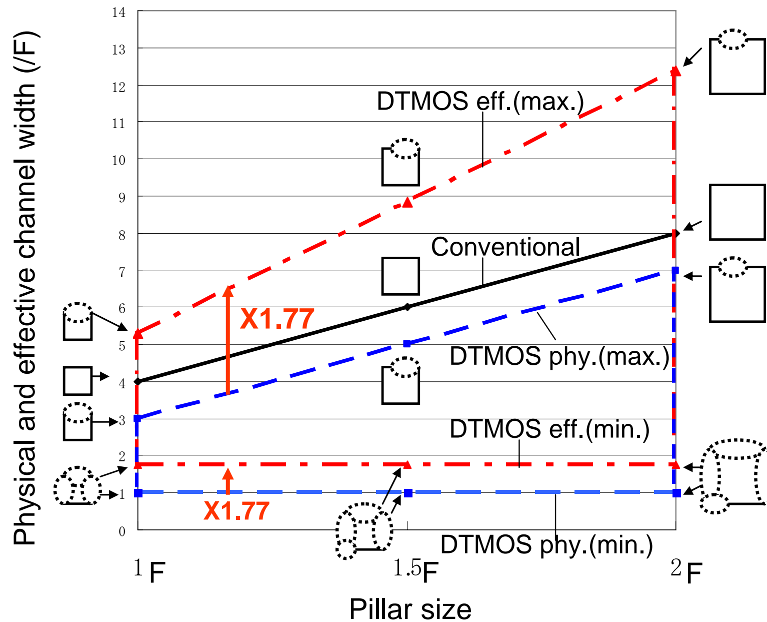

Figure 5: Physical and effective channel width vs silicon pillar size of DTMOS type SGT and conventional SGT.

3 Pattern area and delay time reduction of logic circuit using newly proposed DTMOS type SGT

In the previous section feature of DTMOS type SGT with small channel width reduction rate has been described. In this section the packing density of effective channel width which is normalized with the pattern area of the logic circuit is estimated. The packing density of effective channel width is defined as (5).

(Packing density of effective channel width)
=(Total effective channel width of circuit)/(Pattern area of circuit) ------(5)

The packing density of effective channel width is more accurate than channel width reduction rate for estimation the pattern area and delay time of logic circuit. This is because, the packing density of effective channel width takes into accounts to not only effective channel width of circuit but also pattern area which include contact and wiring region.
This packing density of effective channel width is estimated for various kinds of logic circuit such as inverter and NAND circuit. Two kinds of design rule, relatively relaxed design rule which corresponds to silicon pillar size of 2F*2F and aggresive tight design rule which corresponds to silicon pillar size of F*F, are adopted. Relatively relaxed design rule is shown in Table 1.

Table 1: Relatively relaxed design rule. Silicon pillar size is 2F*2F.

	Planar	Conv.SGT	DTMOS SGT
Gate length	F	F	F
Wiring	F	F	F
Wiring to Wiring (same)	F	F	F
Wiring to Wiring (diff.)	—	0.5F	0.5F
Well isolation	3F	3F	3F
Contact size	F×F	F×F	F×F
Silicon pillar size	—	2F×2F	2F×2F
Gate to contact	—	0.5F	0.5F
AA to silicon pillar	—	0.5F	0.5F
Sidewall contact size	—	—	F×F

Except for the sidewall contact size, design rule of DTMOS type SGT is the same as that of conventional SGT. Gate to contact on the silicon pillar is as large as 0.5F. This relatively relaxed design rule enables to use the conventional photo mask process. As a result, the pillar size becomes as large as 2F*2F. In described in the previous report[9] SGT is effective for LSI with small channel width[17] compared with that of FinFET. Therefore, channel width of the logic circuit estimated in this section is relatively small as follows. For the pattern design of inverter circuit β ratio of 2 is adopted[18]. The pattern of inverter is consisted to one pillar for NMOS and two pillars for PMOS as shown in Fig.6. The pattern of DTMOS type SGT is almost the same as that of conventional SGT. Therefore, the pattern area 5.5F*13F=71.5F^2 of DTMOS type SGT is the same as that of conventional SGT.

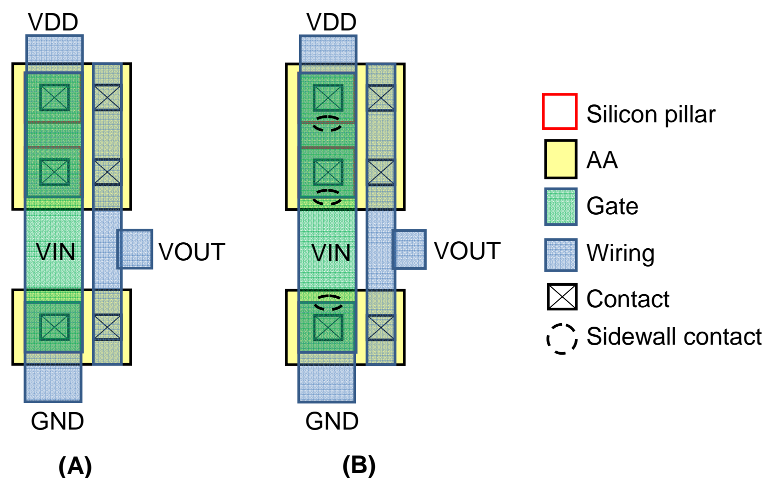

Figure 6: Pattern of inverter with SGT using pillar size of 2F*2F. Pattern area is 5.5F*13F=71.5F^2. (A)Conventional SGT, (B)DTMOS type SGT.

Within this pattern area NMOS of channel width of 8F and PMOS of channel width of 16F is placed for conventional SGT case (Fig.6 (A)). For the DTMOS type NMOS of physical channel width of 7F and PMOS of physical channel width of 14F is placed (Fig.6 (B)). 7F for NMOS and 14F PMOS are maximum physical values corresponding to this pillar size for realizing high speed operation (Fig.5). Using the 1/m=1.77, these values of physical channel width are transferred to 7F*1.77=12.4F and 14F*1.77=24.8F of effective channel width (Fig.5). As a result, using (5) packing density of effective channel width of inverter can be estimated. The value is $0.291F/F^2*1.77=0.515F/F^2$ for DTMOS type SGT and $0.333F/F^2$ for conventional SGT.

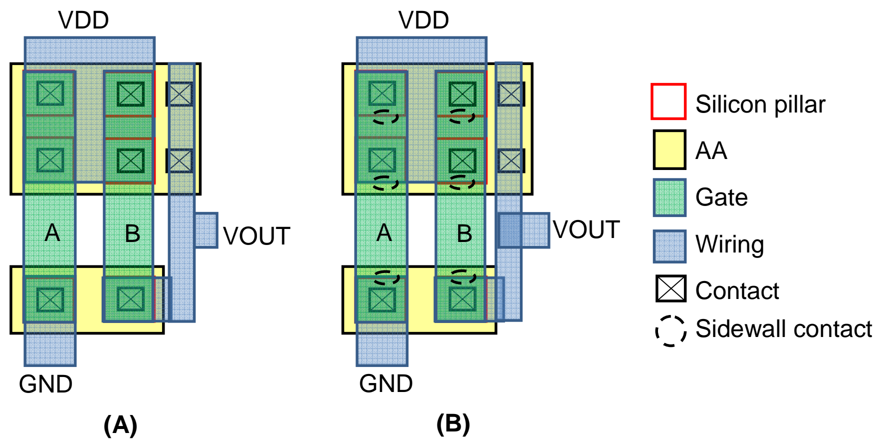

Figure 7: Pattern of 2-input NAND circuit with SGT using pillar size of 2F*2F. Pattern area is $8.5F*13F=110.5F^2$. (A)Conventional SGT, (B)DTMOS type SGT.

The pattern of 2-input NAND with pillar size of 2F*2F is shown in Fig.7. As the same as the inverter circuit the pattern of DTMOS type SGT is almost the same as that of conventional SGT except for sidewall contact. The packing density of effective channel width is $0.380F/F^2*1.77=0.673F/F^2$ for DTMOS type SGT and $0.434F/F^2$ for conventional SGT.
For both conventional and DTMOS type SGT, the packing density of effective channel width of 2-input NAND is larger than that of inverter. This is because, NAND circuit is highly packed pillar structure compared to inverter as shown in Fig.6 and Fig.7.

The aggresive tight design rule which corresponds to silicon pillar size of F*F is shown in Table 2.

Table 2: Aggressive tight design rule. Silicon pillar size is F*F.

	Planar	Conv. SGT	DTMOS SGT
Gate length	F	F	F
Wiring	F	F	F
Wiring to Wiring (same)	F	F	F
Wiring to Wiring (diff.)	—	0.5F	0.5F
Well isolation	3F	3F	3F
Contact size	F×F	F×F	F×F
Silicon pillar size	—	F×F	F×F
Gate to contact	—	0F	0F
AA to silicon pillar	—	0.5F	0.5F
Sidewall contact size	—	—	F×F

Except for the sidewall contact size, design rule of DTMOS type SGT is the same as that of conventional SGT. Gate to contact on the silicon pillar is as small as 0F. This aggressive tight rule leads to use the advanced self-aligned process. As a result, the pillar size can be reduced as small as F*F.

The pattern of inverter with pillar size of F*F is shown in Fig.8. As the same as the pillar size of 2F*2F the pattern of DTMOS type SGT is almost the same as that of conventional SGT except for sidewall contact. The packing density of effective channel width is $0.202F/F^2*1.77=0.358F/F^2$ for DTMOS type SGT and $0.270F/F^2$ for conventional SGT. For both conventional and DTMOS type SGT, the packing density of effective channel width of pillar size of F*F is smaller than that of pillar size of 2F*2F. This is because, pillar size of 2F*2F is highly packed pillar structure compared to pillar size of F*F as shown in Fig.6 and Fig.8. This indicates that the reduction of silicon pillar size of inverter with small channel width results in the reduction of packing density of the effective channel width.

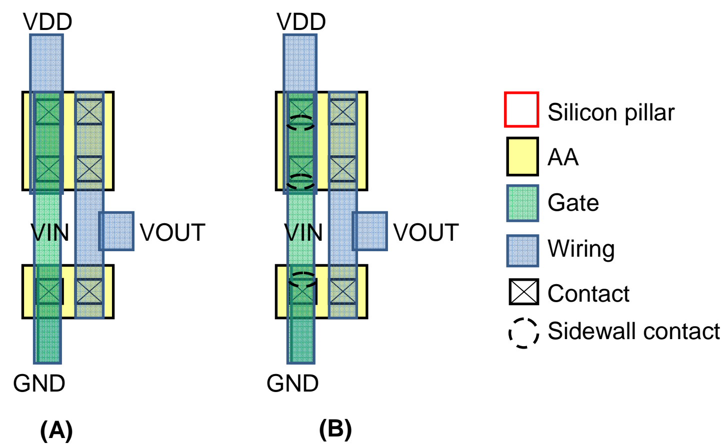

Figure 8: Pattern of inverter with SGT using pillar size of F*F. Pattern area is $4.5F*10F=45F^2$. (A)Conventional SGT, (B)DTMOS type SGT.

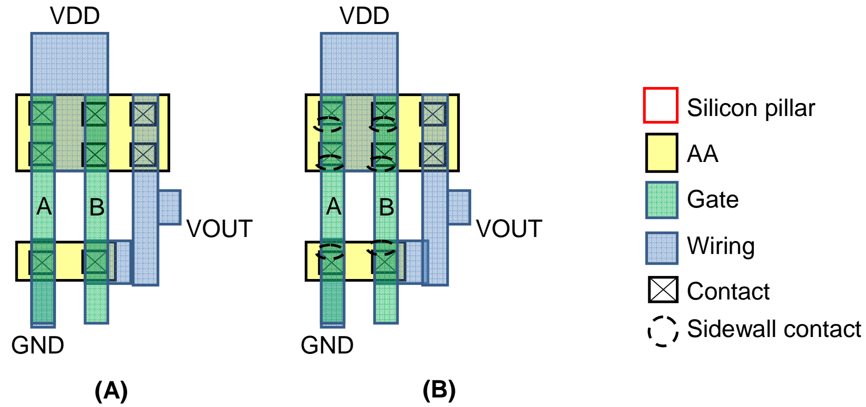

Figure 9: Pattern of 2-input NAND circuit with SGT using pillar size of F*F. Pattern area is 6.5F*10F=65F^2. (A)Conventional SGT, (B)DTMOS type SGT.

The pattern of 2-input NAND with pillar size of F*F is shown in Fig.9. As the same as the pillar size of 2F*2F the pattern of DTMOS type SGT is almost the same as that of conventional SGT except for sidewall contact. The packing density of effective channel width is 0.272F/F^2*1.77=0.481F/F^2 for DTMOS type SGT and 0.369F/F^2 for conventional SGT. For both conventional and DTMOS type SGT, the packing density of effective channel width of pillar size of F*F is smaller than that of pillar size of 2F*2F. This is because, pillar size of 2F*2F is highly packed pillar structure compared to pillar size of F*F as shown in Fig.7 and Fig.9. This indicates that the reduction of silicon pillar size of 2-input NAND with small channel width results in the reduction of packing density of the effective channel width.

Pattern of 3-input NAND and 4-input NAND circuit with pillar size of F*F and 2F*2F, and inverter/2-NAND with pillar size of 1.5F*1.5F are designed and the packing density of effective channel width is estimated. The estimated result is shown in Fig.10. As described in inverter and 2-input NAND, packing density of channel width increases with increasing the pillar size for all estimated circuits. As described in inverter and 2-input NAND, packing density increases with increasing the number of input. For all estimated circuit and pillar size the packing density of effective channel width for DTMOS type SGT is larger than that of conventional SGT. Estimation of this section is about the circuit with small channel width. Therefore, this large packing density of effective channel width is effective for realizing reduction of delay time of logic circuit. Delay time comparison between conventional SGT case and DTMOS type SGT case for various kinds of circuits is shown in Table 3. The delay time of conventional SGT case is set to 1.

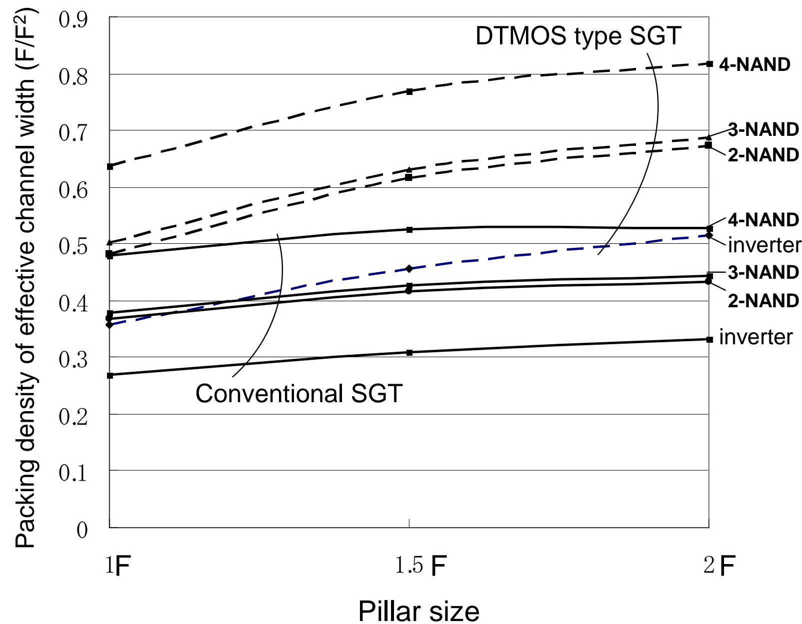

Figure 10: Packing density of effective channel width vs pillar size for inverter and NAND circuit. Both conventional (solid line) and DTMOS type SGT case (dotted line) are estimated.

Table 3: Delay time comparison between conventional SGT case and DTMOS type SGT case for various kinds of circuits. The delay time of conventional SGT case is set to 1.

pillar size	inverter	2-NAND	3-NAND	4-NAND
F*F	0.755	0.766	0.754	0.753
1.5F*1.5F	0.679	0.677	0.678	0.682
2F*2F	0.645	0.645	0.645	0.644

Independent to circuit structure delay time with pillar size of F*F, 1.5F*1.5F, and 2F*2F, can be successfully reduced to 0.75-0.77, 0.67-0.68, and 0.64-0.65, respectively. Therefore, newly proposed DTMOS type SGT is very effective for high speed operation of logic circuit such as inverter and NAND with small channel width compared to conventional DTMOS case.

4 Pattern area and delay time reduction of large channel transistor with DTMOS type SGT

In this section the pattern area and delay time of large channel transistors are compared between conventional and DTMOS type SGT. As described in the previous report[9], large channel width transistor is used for buffer circuit[19] and

cell library[20] such as Data Out. Therefore, the packing density of effective channel width (packing density) of large channel transistor for various size and shape of silicon pillar using conventional or DTMOS type SGT are estimated.

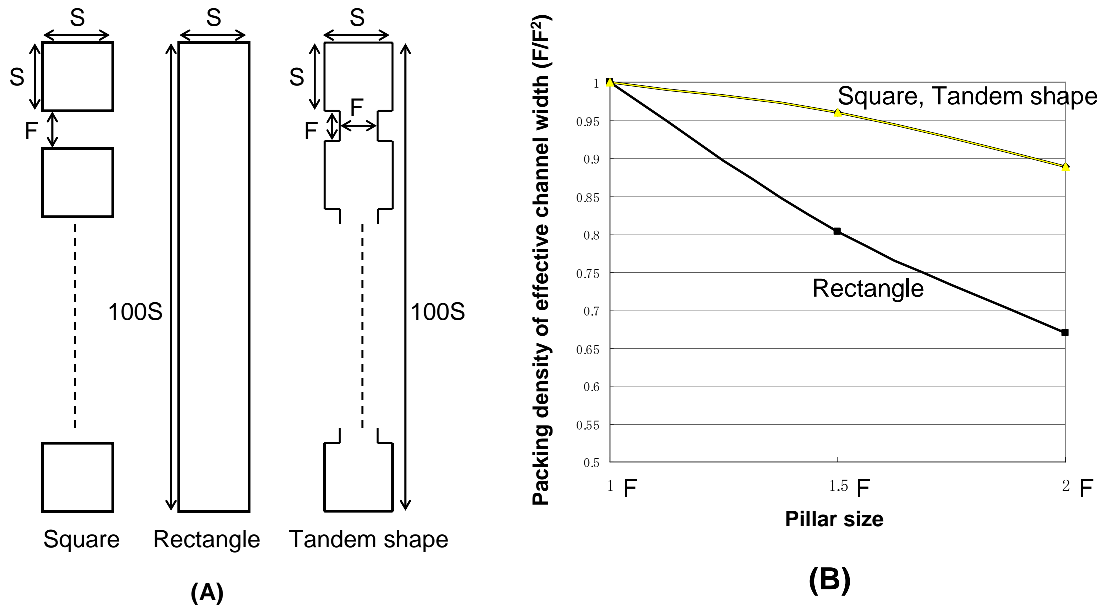

Figure 11: Packing density of effective channel width for long channel transistor with conventional SGT. Pillar size is S*S. (A)Shape of silicon pillar, (B) Packing density of effective channel width vs pillar size.

The packing density of long channel transistor with conventional SGT is shown in Fig.11. The estimated pillar sizes, width of pillar, are F, 1.5F, and 2F. The estimated shapes of pillar are square connected in parallel, rectangle and tandem shape. The maximum length for long side of rectangle and tandem shape are limited to 100*(pillar size) for avoiding the large RC delay of gate electrode[21]. For all shapes the packing density decrease with increasing pillar size. Namely, the reduction of pillar size using tight design rule leads to higher packing density. In the pillar size of F case, the packing density becomes to the same maximum value independent to the shape of pillar. For larger pillar size, the packing density of square in parallel and tandem shape become the same value and the packing density of rectangle is smaller than that of square in parallel and tandem shape. These results shows that by using small pillar size large packing density can be realized independent to the shape of pillar.

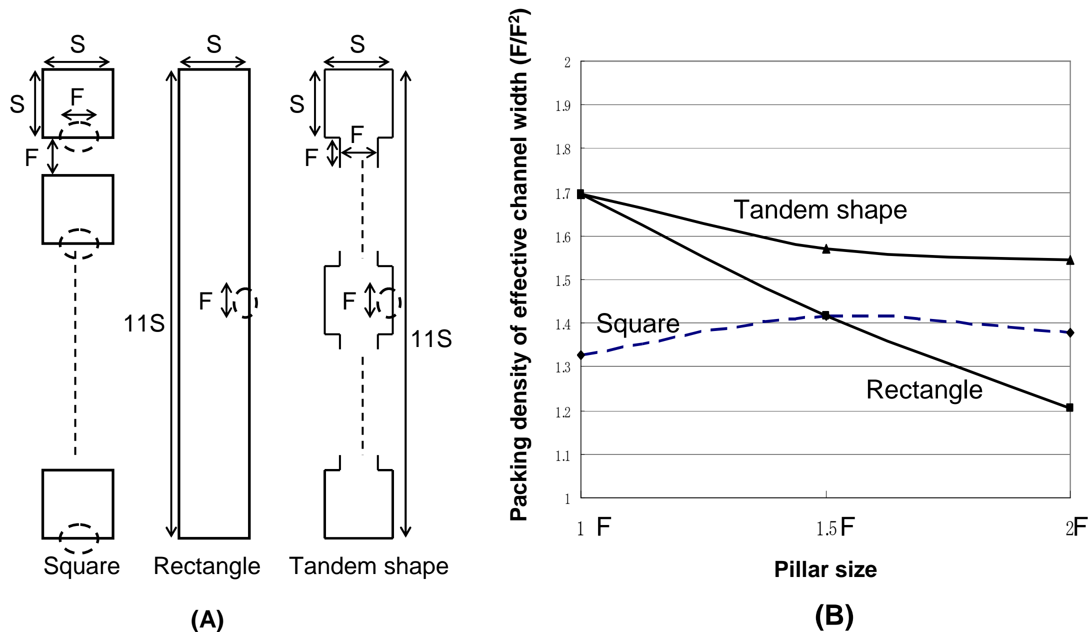

Figure 12: Packing density of effective channel width for long channel transistor with DTMOS type SGT. Pillar size is S*S. (A)Shape of silicon pillar, (B) Packing density of effective channel width vs pillar size.

The packing density of long channel transistor with DTMOS type SGT is shown in Fig.12. The estimated pillar size and shape are the same as conventional SGT case. Sidewall contact must be formed for DTMOS type SGT. Sidewall contact is formed for all squares for square in parallel case and the center of rectangle for rectangle pillar case and center of tandem shape for tandem shape case as shown in Fig.12 (A). The maximum length for long side of rectangle and tandem shape are limited to 11*(pillar size) for avoiding the large RC delay of silicon pillar[14][15]. For rectangle and tandem shape case, the packing density decrease with increasing pillar size as well as conventional SGT case. On the other hand, for square in parallel case the packing density becomes to maximum value with pillar size of 1.5F. This is because, smaller pillar size suffers from large reduction of channel width by the sidewall contact formed to all square pillars. The maximum value of packing density is obtained for both tandem shape and rectangle case with pillar size of F. This is because, the reduction of channel width by the sidewall contact is relatively small for these case. If the tight design rule can not be used, the pillar size must be enlarged to 1.5F-2F. In this case tandem realizes the largest packing density.
From Fig.11 and Fig.12, it is clear that the packing density of effective channel width of DTMOS type SGT is larger than that of conventional SGT for all pillar size and shape of silicon pillar conditions. Therefore, LSI using DTMOS type

SGT can realize high speed characteristic or small pattern area compared to conventional SGT case without sacrificing the power consumption. Using Fig.11 and 12, the reduction rate of delay time or pattern area are estimated. Estimated results are shown in Table 4. Reduction rate is estimated using (packing density with conventional SGT)/(packing density with DTMOS type SGT). The smaller reduction rate means smaller delay time or pattern area. For all shapes the reduction rate decreases with increasing pillar size. For rectangle and tandem shape case the reduction rate is as small as 0.56-0.61. For square in parallel case the reduction rate is relatively large value of 0.65-0.75. This is because sidewall contact for all squares reduces the channel width. For realizing large channel transistor with DTMOS type SGT rectangle and tandem shape is promising candidate.

Table 4: Reduction rate of delay time or pattern area with DTMOS type SGT.

pillar size	Squares	Rectangle	Tandem
F*F	0.75	0.59	0.59
1.5F*1.5F	0.68	0.57	0.61
2F*2F	0.65	0.56	0.58

Although maximum applied voltage is limited to 0.7V of forward bias for PN junction, digital LSI with DTMOS type SGT becomes increasingly important because of low power and high speed characteristics.

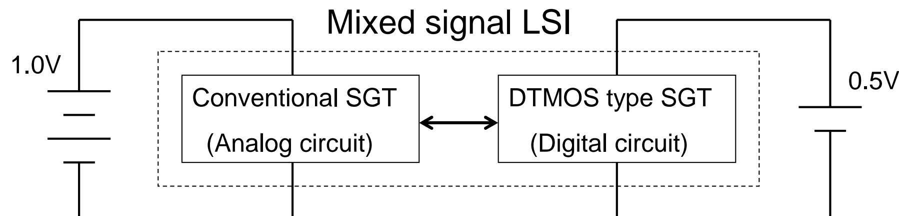

Figure 13: Configuration of mixed signal LSI with conventional and DTMOS type SGT.

On the other hand LSI such as analog application can not operate with low supply voltage below 0.7V. For realizing the mixed signal LSI which are composed with digital part and analog part, the mixed configuration with conventional SGT and DTMOS type SGT as shown in Fig.13 is promising candidate. Digital circuit with newly proposed DTMOS type SGT operates using supply voltage of 0.5V. Analog circuit with conventional SGT operates using supply voltage of 0.5V*2=1.0V (Fig.13). These configuration is promising candidates for realizing future mixed signal LSI.

5 Conclusion

The reduction of pattern area and delay time for logic circuit using newly proposed DTMOS type SGT with the same power consumption compared to that using conventional SGT are described. The reduction of delay time of logic circuit such as inverter and NAND circuit with small channel width using DTMOS type SGT is presented. The delay times of these circuits with DTMOS type SGT can be reduced to 64%-77% compared to that with conventional SGT with supply voltage of 0.5V. Furthermore, using large channel width transistor delay time or channel width with DTMOS type SGT can be reduced to 58%-61% compared to that with conventional SGT using supply voltage of 0.5V. DTMOS type SGT is the promising candidates for realizing high density high speed low power LSI.

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