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Circuit Design of Reconfigurable Dynamic Logic Based on Double Gate CNTFETs Focusing on Number of States of Back Gate Voltages

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Abstract

In this paper circuit design of reconfigurable dynamic logic based on double gate CNTFETs focusing on number of states of back gate voltages has been newly described. 16 function 9-10T DRDLC for two Boolean inputs with two states (+V, -V) of back gate voltages has been newly proposed. Using this 9-10T DRDLC the conventional 7T DRDLC with three states (+V, 0, -V) of back bate voltages is successfully derived. Furthermore, using four states (+2V, +V, 0, -V) of back gate voltages 6T DRDLC can be realized. These DRDLC with small number of DG-CNTFETs is promising candidates for realizing future high performance reconfigurable LSI.

Keywords: reconfigurable logic, ambipolar device, double gate CNTFET

1 Introduction

Recently, the number of transistors and the chip area increases in order to implement the highly developed processing. As a method to reduce the number of

transistors, the double gate (DG) carbon nanotube (CNT) FET which have the ambipolar property is getting some attention[1]. This ambipolar property can be realized using a second gate (polarity gate:PG)[1] in addition to a conventional first gate. The polarity gate PG has the plural states of the back gate voltages and the role to control the DG-CNTFET. Using the DG-CNTFETs, the simple logic with two Boolean inputs has been previously reported.

First report was dynamically reconfigurable dynamic logic circuit (DRDLC) with 9 transistors using two states (+V, -V) of the back gate voltages[1]. If the polarity gate PG is set to +V or –V, then DG-CNTFET works as N-type MOSFET or P-type MOSFET, respectively. Using this circuit 6 logic functions can be realized. DG-CNTFET with two states case has advantage to fabricate DG-CNTFET easily. This is because the threshold voltage and leakage current control concerning about the back gate voltage of 0V is not required for this case. However, this value of 6 is too small compared to 2^4=16 which is required for two Boolean input circuit. DRDLC which generate the whole set of 16 functions using two states of the back gate voltages has not been reported.

Recently, for realizing 16 functions new type DRDLC with only 7 transistors using three states (+V, 0, -V) of the back gate voltages was reported[2]. In ref[2] second states of “0” is used for realizing the off state of DG-CNTFET. The fabrication of DG-CNTFET with three states of the back gate voltages can be realized with rather complicated process technology compared to that with two states cases. This is because the threshold voltage and leakage current control about the back gate voltage of 0V become very important for this case. Furthermore, advanced technology, DRDLC using four states of the back gate voltages, has not been reported.

In this paper circuit design of DRDLC with two Boolean inputs focusing on the number of states of back gate voltage has been newly described. In this design without sacrificing the logic functions of 16 numbers of transistors is reduced as small as possible.

This paper is organized as follows. In section 2 new type DRDLC with only 9-10 transistors using two states (+V, -V) of back gate voltages has been newly proposed. In section 3, the configuration of previously proposed DRDLC with 7 transistors using three states (+V, 0, -V) of back gate voltages is derived from two states scheme described in section 2. In section 4, new type DRDLC with only 6 transistors using four states (+2V, +V, 0, -V) of the back gate voltages with 16 functions has been newly proposed. This scheme is derived from three states scheme described in section 3. Finally, a conclusion of this work is provided in Section 5.

2 New type DRDLC with only 9-10 transistors using two states (+V, -V) of back gate voltages

In section 2, firstly, 6 function DRDLC with 9 transistors using two states (+V, -V) of the back gate voltages[1] has been described. After that, new type 16

function DRDLC with only 9-10 transistors using two states (+V, -V) of back gate voltages has been newly proposed.
Conventional 6 function DRDLC with 9 transistors using two states (+V, -V) of the back gate voltages[1] is shown in Fig.1. This circuit has two boolean data inputs (A and B), three configuration inputs (OP1, OP2, OP3), and four clock inputs (EV1, PC1, PC2, EV2) and one output of Y. In this figure, each transistor consists of a DG-CNTFET and configuration inputs (OP1, OP2, OP3) have two states (+V, -V) of back gate voltages. These configuration input control DG-CNTFET as N-type configuration for +V, and the P-type configuration for –V as shown in Fig.2. Four clock inputs (EV1, PC1, PC2, EV2) have the role of the dynamic logic style[3] used in this circuit. Finally, the output of circuit Y is decided as 0 and +V by Boolean inputs A and B. In this way, configuration inputs (OP1, OP2, OP3) determine the logic function realized by the circuit in Fig.1. Table 1 shows the configuration inputs and the corresponding logic function of Y.

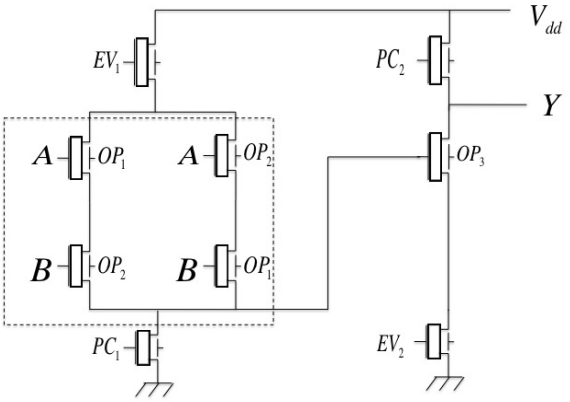

Figure 1: Conventional 6-function 9T DRDLC with two state (+V, -V).

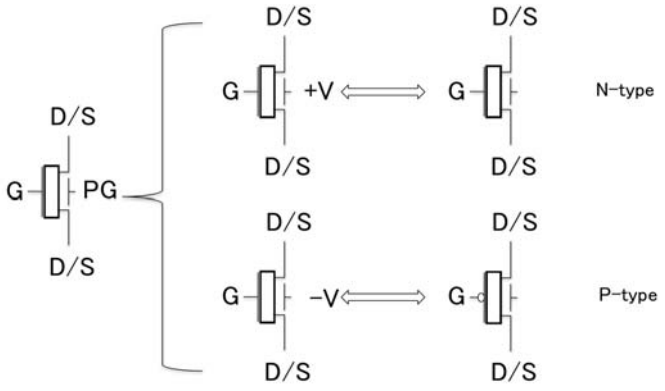

Figure 2: DG-CNTFET device symbol and configurations with two state (+V, -V).

Table 1: Configuration inputs and corresponding logic functions for conventional 6-function 9T DRDLC with two state (+V, -V).

OP_1	OP_2	OP_3	Y	
+V	+V	+V	$\overline{A}\cdot\overline{B}$	6 Functions
+V	+V	−V	$A\cdot B$	
+V	−V	+V	$\overline{A\oplus B}$	
+V	−V	−V	$A\oplus B$	
−V	+V	+V	$\overline{A\oplus B}$	
−V	+V	−V	$A\oplus B$	
−V	−V	+V	$A+B$	
−V	−V	−V	$\overline{A+B}$	

6 functions can be realized with 9 transistors. The circuit block shown by the broken line in Fig.1 is very effective for generating logical conjunction of two Boolean function such as AB and $\overline{A}\,\overline{B}$ or product-sum operation of two Boolean function such as (A XOR B) and (A XNOR B). This is because two DG-CNTFET connected in series generates logical conjunction and DG-CNTFET connected in parallel generates logical sum operation. However, this conventional DRDLC can realize only 6 functions which is too small compared to 16 functions. Therefore, the conventional DRDLC can be used to the limited application such as full adder circuit[1].

In order to overcome this limitation 10T DRDLC which can generate 16 functions has been newly proposed. Newly proposed DRDLC is shown in Fig.3. This circuit consists with 10 transistors using two states (+V, -V), eight configuration inputs (C1-C8), and two clock inputs (EV, PC). Table 2 shows the configuration inputs and the corresponding inputs and corresponding logic function of $\overline{F}$.

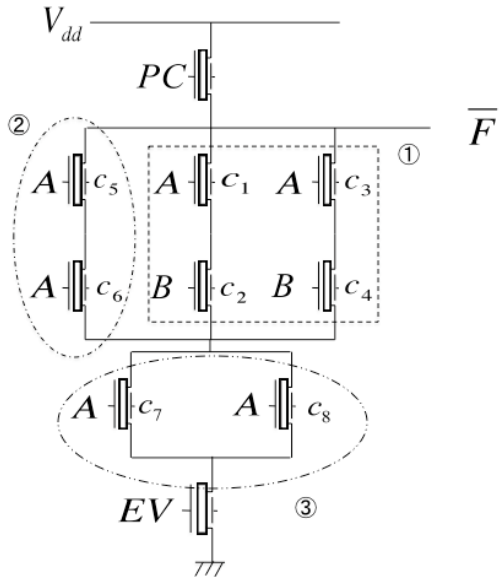

Figure 3: Newly proposed 16-function 10T DRDLC with two state (+V, -V).

Table 2: Configuration inputs and corresponding logic functions for newly proposed 16-function 10T DRDLC with two state (+V, -V).

c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	F
+V	+V	+V	+V	+V	−V	+V	−V	AB
−V	−V	−V	−V	+V	−V	+V	−V	$\overline{A+B}$
+V	−V	+V	−V	+V	−V	+V	−V	$A\overline{B}$
−V	+V	−V	+V	+V	−V	+V	−V	$\overline{A}B$
−V	+V	+V	−V	+V	−V	+V	−V	$A \oplus B$
−V	−V	+V	+V	+V	−V	+V	−V	$\overline{A \oplus B}$
+V	+V	−V	+V	+V	−V	+V	−V	B
+V	−V	−V	−V	+V	−V	+V	−V	$\overline{B}$
+V	+V	+V	−V	+V	−V	+V	−V	A
−V	+V	−V	−V	+V	−V	+V	−V	$\overline{A}$
+V	+V	−V	+V	+V	+V	+V	−V	$A+B$
+V	−V	−V	−V	+V	+V	+V	−V	$A+\overline{B}$
+V	+V	−V	+V	−V	−V	+V	−V	$\overline{A}+B$
+V	−V	−V	−V	−V	−V	+V	−V	$\overline{A}+\overline{B}$
+V	+V	+V	−V	+V	+V	−V	−V	$\perp$
+V	+V	+V	−V	−V	−V	+V	+V	T

As shown in conventional DRDLC of Fig.1 circuit block within circle of broken line is very effective for generating various kinds of Boolean logic. Therefore, in the newly proposed DRDLC modified circuit block of this circuit indicated with ① in Fig.3 is adopted. Furthermore, circuit block ② which is connected to ① in parallel and circuit block ③ which is connected to circuit block ①/② in series are newly introduced. Circuit block ② and ③ are required to generate 16 functions.

16 functions are consisted with logical conjunction of two Boolean inputs (AB, $\overline{A+B}$, $A\overline{B}$, $\overline{A}B$), product-sum of two Boolean inputs (A XOR B, A XNOR B), logic which depends on only A or B (A, $\overline{A}$, B, $\overline{B}$), sum of two Boolean inputs (A+B, $\overline{A}$+B, A+$\overline{B}$, $\overline{A}+\overline{B}$), and logic which is independent to two Boolean inputs ("1", "0"). By using circuit block ① 10 functions can be generated. That is, logical conjunction of two Boolean inputs of 4 functions such as AB+AB=AB, product-sum of two Boolean inputs of 2 functions such as A$\overline{B}$+$\overline{A}$B=A XOR B, and logic which depends on only A or B of 4 functions such as AB+$\overline{A}$B=(A+$\overline{A}$)B=B.

Residual 16-10=6 functions can not be generated with only circuit block ①. For realizing the residual functions circuit block ② is used together with circuit block ①. Circuit block ② is consisted with two DG-CNTFET connected in series. The Boolean input of this DG-CNTFET is the same logic of A, and the configuration inputs are different signal of C5 and C6. By using circuit block ① and ②, sum of two Boolean inputs of 4 functions can be generated. For example, logic of B which is generated by circuit block ① using AB+$\overline{A}$B=B(A+$\overline{A}$)=B and AA=A generated by circuit block ② realizes A+B. Furthermore, "1" which is independent to two Boolean inputs can be generated as follows. That is, AB+A$\overline{B}$=A(B+$\overline{B}$)=A generated by circuit block ① and $\overline{A}\overline{A}=\overline{A}$ generated by circuit block ② realizes A+$\overline{A}$="1". For generating 10 functions which can be realized with only circuit block ①, circuit block ② must be off state. For realizing off state $A\overline{A}$="0" is generated within circuit block ②. This Boolean operation $A\overline{A}$ = "0" is indispensable for realizing off state for 2 states (+V, -V) case. This is because, off state can not be realized with only one DG-CNTFET for 2 states (+V, -V) case. For generating 10+4+1=15 functions which can be realized with only circuit block ① and ②, circuit block ③ must be on state. Circuit block ③ is consisted with two DG-CNTFET connected in parallel. The Boolean inputs of these DG-CNTFET are the same value of A. For realizing on state of circuit block ③, $A+\overline{A}$="1" is indispensable. This is because, on state can not be realized with only one DG-CNTFET for 2 states (+V, -V) case.

Residual function of "0" can not be generated with only circuit block of ① and ②. For realizing "0" circuit block ③ is used together with circuit block of ① and ②. Circuit block ③ and circuit block ①/② is connected in series as shown in Fig.3. $AB+A\overline{B}$=A(B+$\overline{B}$)=A generated by circuit block ① and

$\overline{A}+\overline{A}=\overline{A}$ generated by circuit block ③ realizes $A\overline{A}$="0". As described above, circuit block ② which realizes off state and circuit block ③ which realizes on state are indispensable for 2 states (+V, -V) case.

Furthermore, for more reduction of number of transistors circuit block ③ can be replaced by one DG-CNTFET as shown in Fig.4, if the input of configuration as Boolean logic can be allowed. In this case the number of transistors can be successfully reduced to 9 which is the same number of conventional 6-function 9T DRDLC. Configuration inputs and corresponding logic functions for newly proposed 16-function 9T DRDLC with two state (+V, -V) is shown in Table 3.

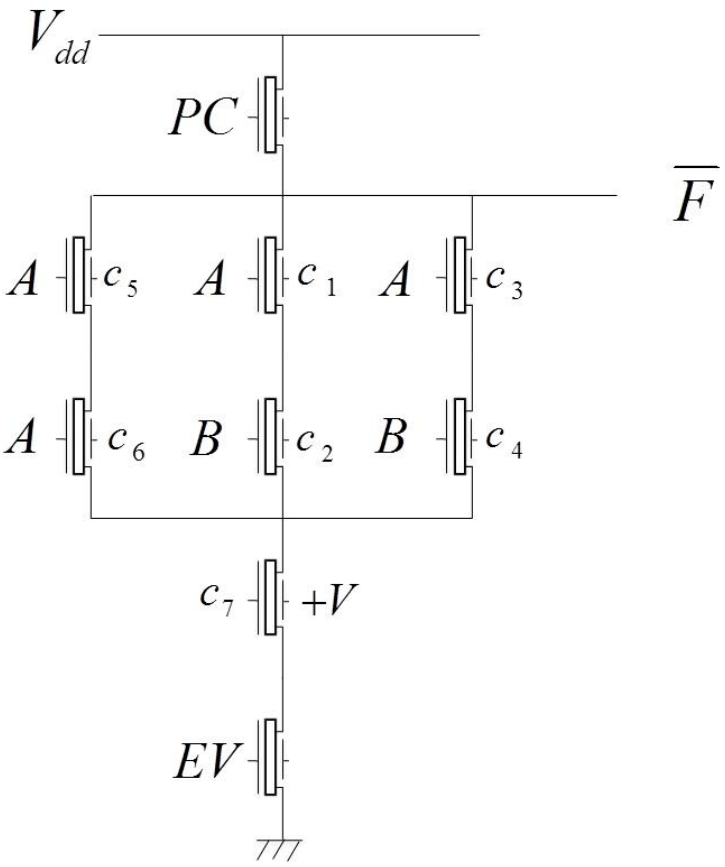

Figure 4: Newly proposed 16-function 9T DRDLC with two state (+V, -V).

Table 3: Configuration inputs and corresponding logic functions for newly proposed 16-function 9T DRDLC with two state (+V, -V).

c_1	c_2	c_3	c_4	c_5	c_6	c_7	F
+V	+V	+V	+V	+V	−V	V	AB
−V	−V	−V	−V	+V	−V	V	$\overline{A+B}$
+V	−V	+V	−V	+V	−V	V	$A\overline{B}$
−V	+V	−V	+V	+V	−V	V	$\overline{A}B$
−V	+V	+V	−V	+V	−V	V	$A \oplus B$
−V	−V	+V	+V	+V	−V	V	$\overline{A \oplus B}$
+V	+V	−V	+V	+V	−V	V	B
+V	−V	−V	−V	+V	−V	V	$\overline{B}$
+V	+V	+V	−V	+V	−V	V	A
−V	+V	−V	−V	+V	−V	V	$\overline{A}$
+V	+V	−V	+V	+V	+V	V	$A+B$
+V	−V	−V	−V	+V	+V	V	$A+\overline{B}$
+V	+V	−V	+V	−V	−V	V	$\overline{A}+B$
+V	−V	−V	−V	−V	−V	V	$\overline{A}+\overline{B}$
+V	+V	+V	−V	−V	−V	V	T
+V	+V	+V	−V	−V	−V	−V	$\perp$

3 Derivation of conventional 7T DRDLC using three states (+V, 0, -V) from newly proposed two states (+V, -V) scheme

Conventional 7T DRDLC[2] with three states (+V, 0, -V) can be derivated from the newly proposed 16-function 10T DRDLC with two state (+V, -V) described in section 2. DG-CNTFET device symbol and configurations with three state (+V, 0, -V) is shown in Fig.5. For three states case circuit block ① of two states case is adopted. If there are functions which can not be generated using circuit block ①, modified circuit bock ② and ③ for three states case are introduced as follows.

For three states case using “0” states the off condition of circuit block ① can be easily realized. This is the feature of circuits with three states case which can not be easily realized for circuits with two states case. Therefore, without circuit block ③ function of “0” can be easily generated for 3 states case. Furthermore, using “0” states of one DG-CNTFET the off condition can be easily realized. As a result, circuit block ② can be modified from two DG-CNTFETs connected in series to only one DG-CNTFET. Of cource, the residual 15 function can be successfully realized with parallel connection circuit block ① and one DG-CNTFET corresponding circuit block ② using three states case. As a result, 16 functions can be generated using DRDLC with only 7 transistors as shown in Fig.6. Fig.6 corresponds to ref[2]. Configuration inputs and corresponding logic functions for

conventional 16-function 7T DRDLC with three state (+V, 0, -V) is shown in Table 4. From these deviation conventional 7T DRDLC[2] with three states (+V, 0, -V) can be drived from the newly proposed 16-function 10T DRDLC with two state (+V, -V) described in section 2.

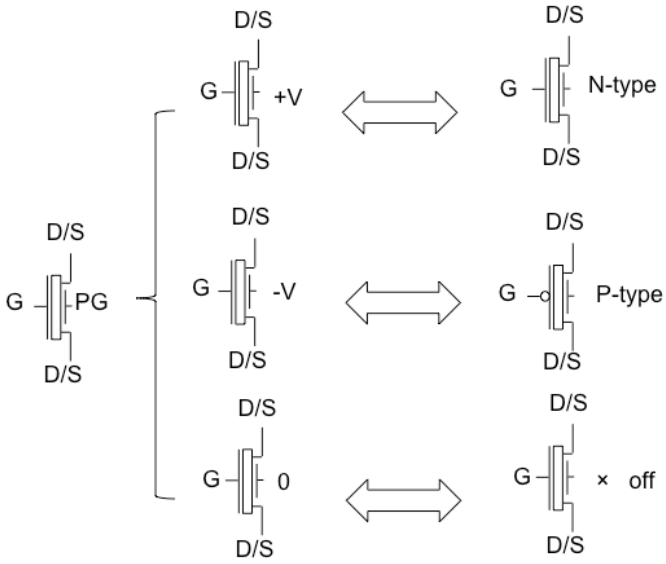

Figure 5: DG-CNTFET device symbol and configurations with three state (+V, 0, -V).

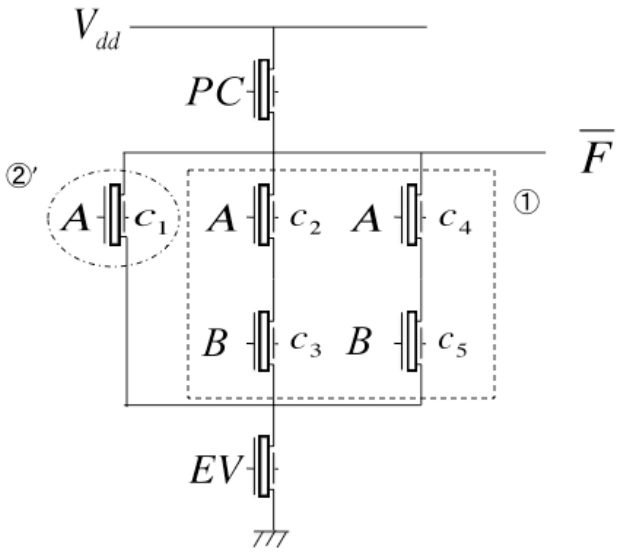

Figure 6: Conventional 16-function 7T DRDLC with three state (+V, 0, -V).

Table 4: Configuration inputs and corresponding logic functions for conventional 16-function 7T DRDLC with three state (+V, 0, -V).

c_1	c_2	c_3	c_4	c_5	F
0	+V	+V	−V	0	AB
0	+V	0	−V	−V	$\overline{A+B}$
0	+V	−V	−V	0	$A\overline{B}$
0	+V	0	−V	+V	$\overline{A}B$
0	+V	+V	−V	−V	$A \oplus B$
0	+V	−V	−V	+V	$\overline{A \oplus B}$
0	+V	+V	−V	+V	B
0	+V	−V	−V	−V	$\overline{B}$
+V	+V	0	−V	0	A
−V	+V	0	−V	0	$\overline{A}$
+V	+V	+V	−V	+V	$A+B$
+V	+V	−V	−V	−V	$A+\overline{B}$
−V	+V	+V	−V	+V	$\overline{A}+B$
−V	+V	−V	−V	−V	$\overline{A}+\overline{B}$
+V	−V	+V	−V	−V	T
0	+V	0	−V	0	$\perp$

4 Newly proposed 6T DRDLC using four states (+2V, +V, 0, -V) of back gate voltages

In section 3 the increase in the number of states for back gate voltages from two to three enable to reduce the number of transistor from 9 to 7 for realizing 16 functions. If the number of states can be increased from three to four, further reduction of number of transistors will be expected. For the conventional double gate MOS transistor on state can be realized independent to Boolean input, if large positive voltage such as +2V is applied to back gate[4][5][6]. It is assumed that this can be realized for DG-CNTFET in this section. In this case DG-CNT device with four state (+2V, +V, 0, -V) can be realized. DG-CNTFET device symbol and configurations with four state (+2V, +V, 0, -V) is shown in Fig.7.

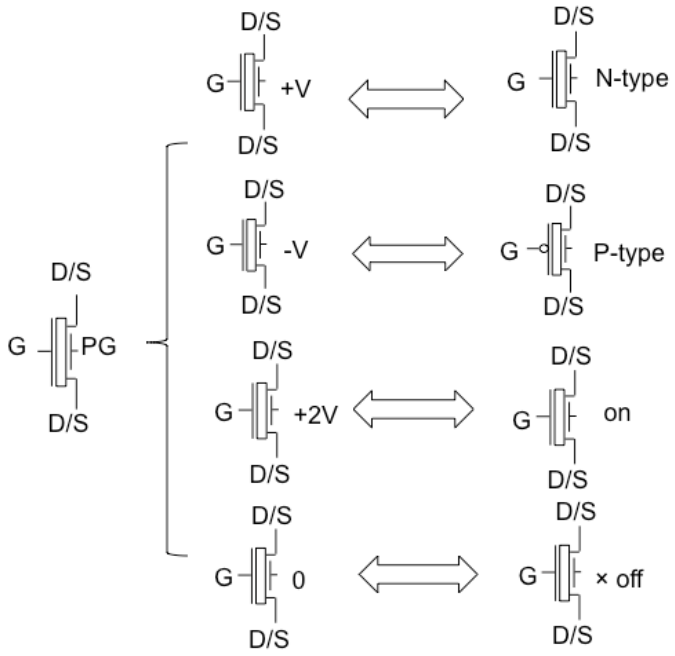

Figure 7: DG-CNTFET device symbol and configurations with four state (+2V, +V, 0, -V).

In this section 6T DRDLC using four state (+2V, +V, 0, -V) of back gate voltages is newly introduced as follows.

For four states case circuit block ① of three states case is adopted. In three states case sum of two Boolean inputs of 4 functions can not be generated within circuit block ①. This is because short of DG-CNTFET can not be realized for three states case. On the other hand short of DG-CNTFET can be easily realized using +2V of back gate voltages for four states case. Therefore, sum of two Boolean inputs of 4 function can be successfully realized with circuit block ① for four state case. Furthermore, logic "1" can be realized using newly introduced +2V of back gate voltages. As a result, 16 functions can be successfully realized with only circuit block ①. This leads to the reduction of number of transistors from 7 for three states case to 6 for four states case as shown in Fig.8. Configuration inputs and corresponding logic functions for newly proposed 16-function 6T DRDLC with four state (+2V, +V, 0, -V) is shown in Table 5.

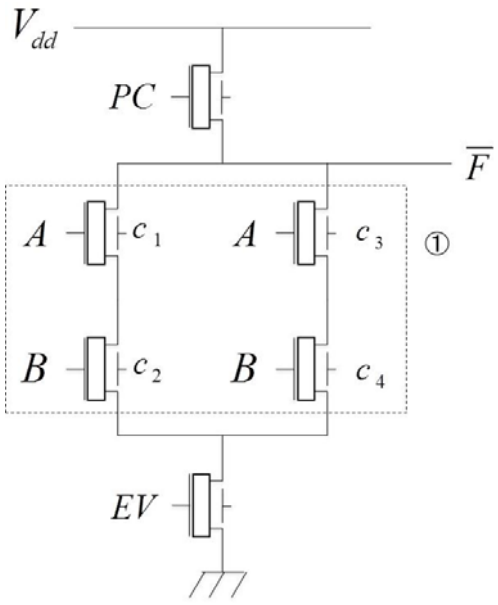

Figure 8: Newly proposed 16-function 6T DRDLC with four state (+2V, +V, 0, -V).

Table 5: Configuration inputs and corresponding logic functions for newly proposed 16-function 6T DRDLC with four state (+2V, +V, 0, -V).

c_1	c_2	c_3	c_4	F
+V	+V	+2V	+2V	AB
-V	-V	+2V	+2V	$\overline{A+B}$
+V	-V	+2V	+2V	$A\overline{B}$
-V	+V	+2V	+2V	$\overline{A}B$
-V	+V	+V	-V	$A \oplus B$
-V	-V	+V	+V	$\overline{A \oplus B}$
+2V	+V	+2V	+2V	B
+2V	-V	+2V	+2V	$\overline{B}$
+V	+2V	+2V	+2V	A
-V	+2V	+2V	+2V	$\overline{A}$
+V	+2V	+2V	+V	$A+B$
+V	+2V	+2V	-V	$A+\overline{B}$
-V	+2V	+2V	+V	$\overline{A}+B$
-V	+2V	+2V	-V	$\overline{A}+\overline{B}$
+V	+2V	-V	+2V	T
0	+2V	0	+2V	$\perp$

4 Conclusion

Circuit design of reconfigurable dynamic logic based on double gate CNTFETs focusing on number of states of back gate voltages has been newly described. 16 function 9-10T DRDLC for two Boolean inputs with two states (+V, -V) of back gate voltages has been newly proposed. Using this 9-10T DRDLC the conventional 7T DRDLC with three states (+V, 0, -V) of back bate voltages is successfully derived. Furthermore, using four states (+2V, +V, 0, -V) of back gate voltages 6T DRDLC can be realized. The concept of newly proposed DRDLC can be used to not only dynamic logic circuit but also static logic circuit[7][8], flip-flop circuit[9] and ALU[10]. These DRDLC with small number of DG-CNTFETs is promising candidates for realizing future high performance reconfigurable LSI.

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