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Analysis of Bit Cost for Stacked Type MRAM with NAND Structured Cell

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Abstract

In this paper the analysis of bit cost of stacked type MRAM with NAND structured cell has been newly described. Both stacked plane and BiCS architecture is very effective for realizing small bit cost of memory cell array. The reduction rate of bit cost for BiCS is larger with larger yield of Y. The reduction rate of bit cost without WBL is larger than that of with WBL. This is because cell size without WBL is smaller than that with WBL for BiCS case, and number of process steps without WBL is smaller than that with WBL for stacked plane case. For more accurate estimation of bit cost not only pattern area of memory cell array but also row decoder should be taken into account. Both stacked plane and BiCS architecture is promising candidates for realizing low cost and high speed non-volatile semiconductor memory.

Keywords: MRAM, NAND structured cell, spin transistor, BiCS, bit cost

1 Introduction

DRAM is widely used for the main memory of personal computer because of its high speed characteristics. On the other hands, NAND flash memory which has the features of non-volatility and low bit cost is widely used for the storage device of the multi-media data. Universal memory which has both features, DRAM and NAND flash memory, is key technology for the future memory system. Recently, two types of stacked type MRAM with NAND structured cell have been proposed for the candidate of the universal memory [1][2][3]. By using spin transistor [4] for memory cell, the magnetic writing scheme generated by a current flow in perpendicular running write bit line and word line (Fig.1(A)) [1] and thermally assisted magnetic writing scheme which use the small heating current of bit line and small current flow of word line (Fig.1(B))[2] have been introduced.

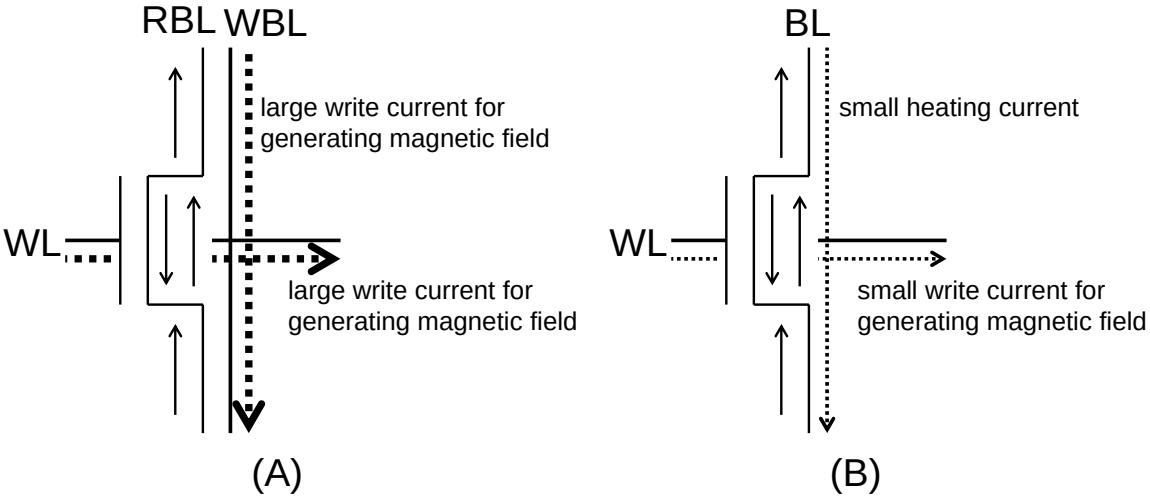

Figure 1: Writing scheme of two types of stacked type MRAM, (A)scheme of ref [1], (B) scheme of ref [2].

In the previous works[1][2][3], the memory cell / core circuit design inherent to the stacked type MRAM with NAND structured cell and performance (the access time) have been described. However, the analysis of bit cost has not been reported.

In this paper the analysis of bit cost of stacked type MRAM with NAND structured cell has been newly described. This paper is organized as follows. Section 2 describes the analysis of bit cost of memory cell array of stacked type NAND MRAM. Section 3 presents the analysis of bit cost not only memory cell array but also core circuit such as row decoder. Finally, a conclusion of this work is provided in Section 4.

2 Analysis of bit cost of memory cell array for stacked type MRAM with NAND structured cell

For memory device the memory cell array occupied almost area of the chip (more than 50%). Therefore, the bit cost of the memory cell array has been estimated in section 2. For estimating the bit cost of stacked type MRAM with NAND structured cell, not only BiCS structure[5][6] proposed by ref [1][2][3] but also stacked horizontal plane structure have been adopted. This stacked type NAND MRAM with the stacked horizontal plane structure has been newly considered for verifying the effectness of BiCS structure compared with stacked horizontal plane structure. For formation of the stacked horizontal plane structure stacked type PRAM with stacked horizontal plane structure is adopted [7]. The stacked horizontal plane structures are designed for both scheme of ref[1] (with WBL) and of ref[2] (without WBL).

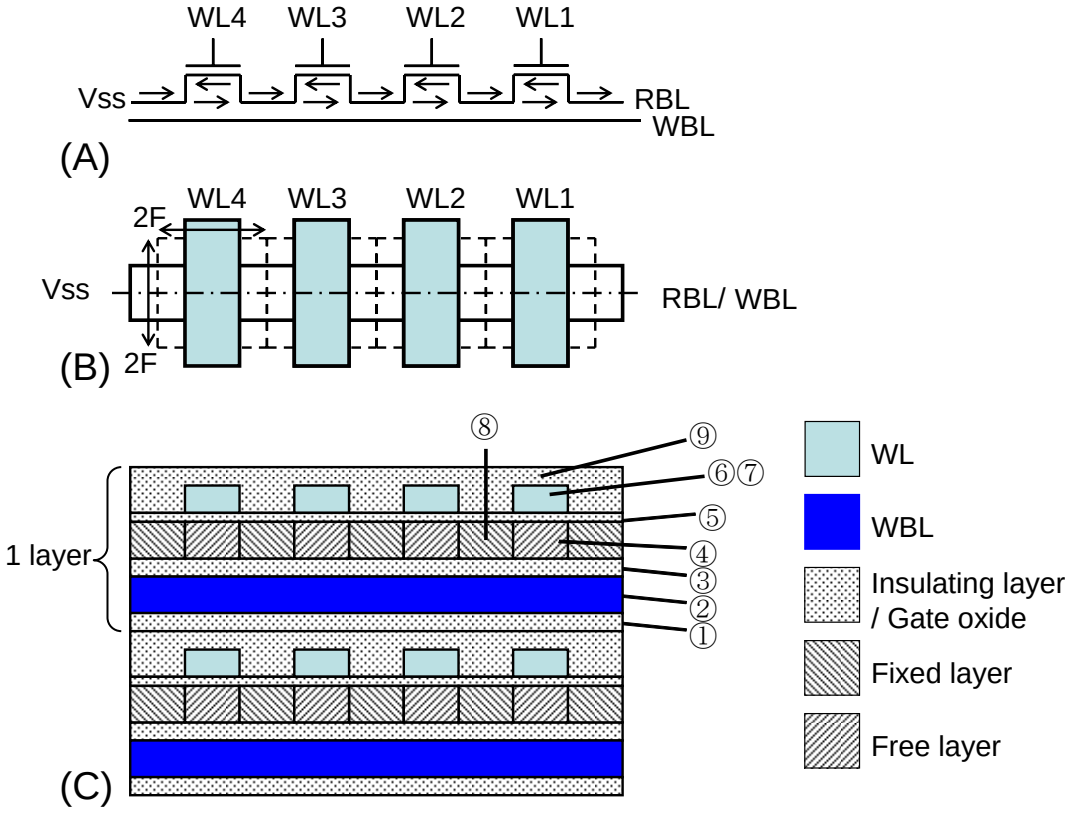

Figure 2: View of stacked type NAND MRAM memory cell array with WBL using stacked horizontal plane structure, (A)Equivalent circuit, (B) Top view, (C)Cross- sectional view.

The view of stacked type NAND MRAM memory cell array with WBL using the stacked horizontal plane structure is shown in Fig.2. 4 memory cells are connected in series for simplicity. The equivalent circuit is shown in Fig.2(A). The top view of memory cell array is shown in Fig.2(B). Spin transistor and WBL are stacked vertically for reducing the memory cell size. This leads to the reduction of memory cell size to $2F*2F=4F^2$ which is smaller than that of BiCS structure with WBL of $9F^2$. The cross sectional view of Fig.2(B) along the broken line is shown in Fig.2(C). The stacked horizontal plane structure is fabricated repeating the formation of one layer horizontal plane structure. In this figure 2 layers are stacked for simplicity. For fabricating one layer horizontal plane structure, 9 process steps should be adopted. That is, ①Formation of insulating layer under WBL, ②Fabrication of WBL, ③Formation of insulating layer under spin transistor, ④Fabrication of free layer for storing memory data, ⑤Fabrication of the gate dielectric, ⑥Formation of gate electrode, ⑦Removal of gate electrode for source and drain region, ⑧Fabrication of fixed layer for source and drain region, ⑨Formation of insulating layer for passivation (Fig.2(C)). For realizing N layers, 9N process steps are required.

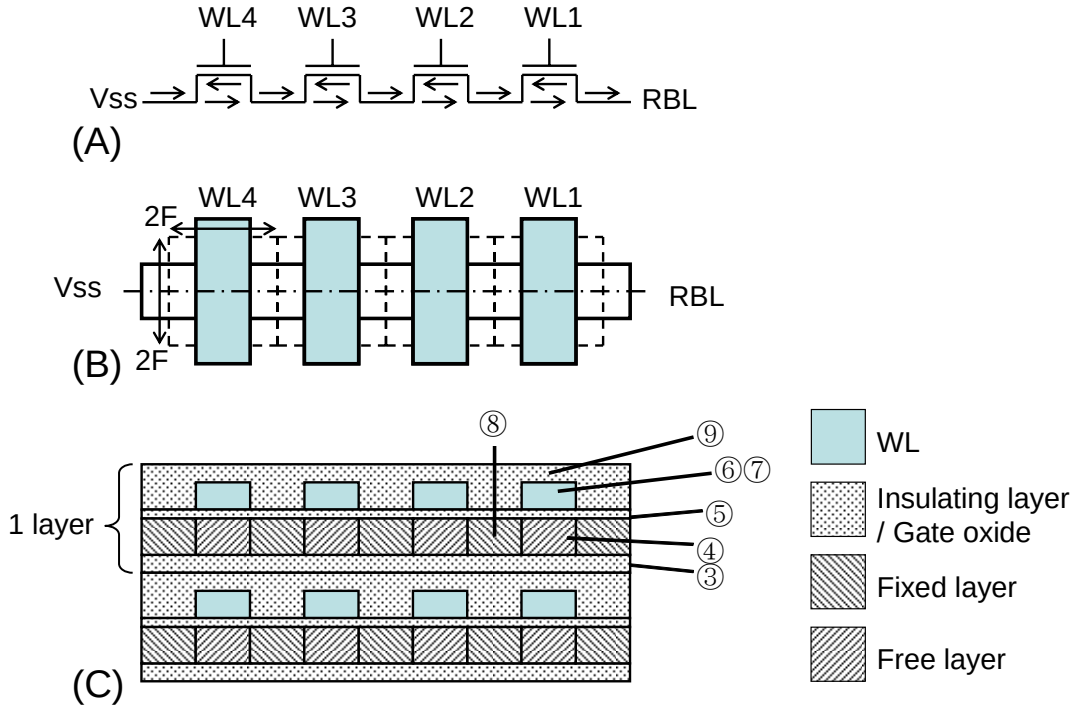

Figure 3: View of stacked type NAND MRAM memory cell array without WBL using stacked horizontal plane structure, (A)Equivalent circuit, (B) Top view, (C)Cross- sectional view.

The view of stacked type NAND MRAM memory cell array without WBL using the stacked horizontal plane structure is shown in Fig.3. 4 memory cells are connected in series for simplicity. The equivalent circuit is shown in Fig.3(A). The top view of memory cell array is shown in Fig.3(B). Only spin transistor is fabricated. The memory cell size is the same as Fig.2(B) of $2F*2F=4F^2$. The cross sectional view of Fig.3(B) along the broken line is shown in Fig.3(C). The stacked horizontal plane structure is fabricated repeating the formation of one layer horizontal plane structure. In this figure 2 layers are stacked for simplicity. For fabricating one layer horizontal plane structure, 7 process steps should be adopted. These steps correspond to ③-⑨ of Fig.2(C). This value is 2 steps smaller than that of Fig.2(C). This is because WBL is not needed for Fig.3(C). For realizing N layers, 7N process steps are required.

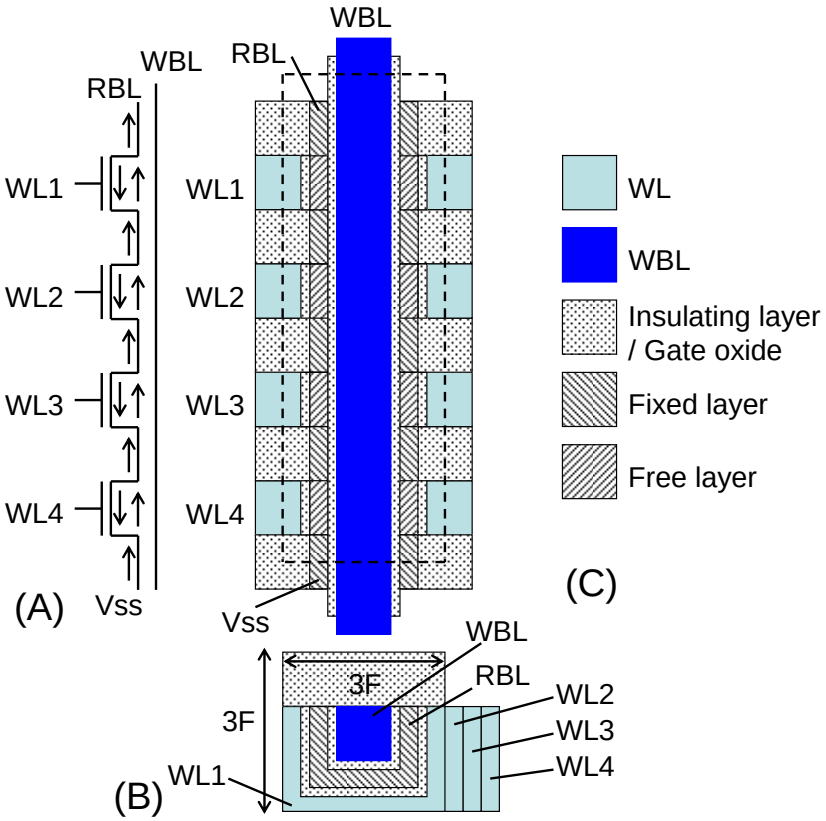

Figure 4: View of stacked type NAND MRAM memory cell array with WBL using BiCS structure, (A)circuit diagram, (B)top view, (C)cross-sectional view.

The view of stacked type NAND MRAM memory cell array with WBL using BiCS structure is shown in Fig.4. 4 memory cells are connected in series for simplicity. The circuit diagram(Fig.4(A)), top view(Fig.4(B)), and cross-sectional view (Fig.4 (C)) are shown in this figure. The memory cell size is $3F*3F=9F^2$. This value is larger than that of stacked horizontal plane structure. This is because both spin transistor and WBL must be designed within the same horizontal plane.

As shown in Fig.4 a NAND structure is fabricated in a vertical direction to the horizontal plane. For realizing this BiCS structure with N layer, after the formation N layers of the insulating layer and WLs, 9 additional process steps shown in Fig.5(A) –(I) should be adopted.

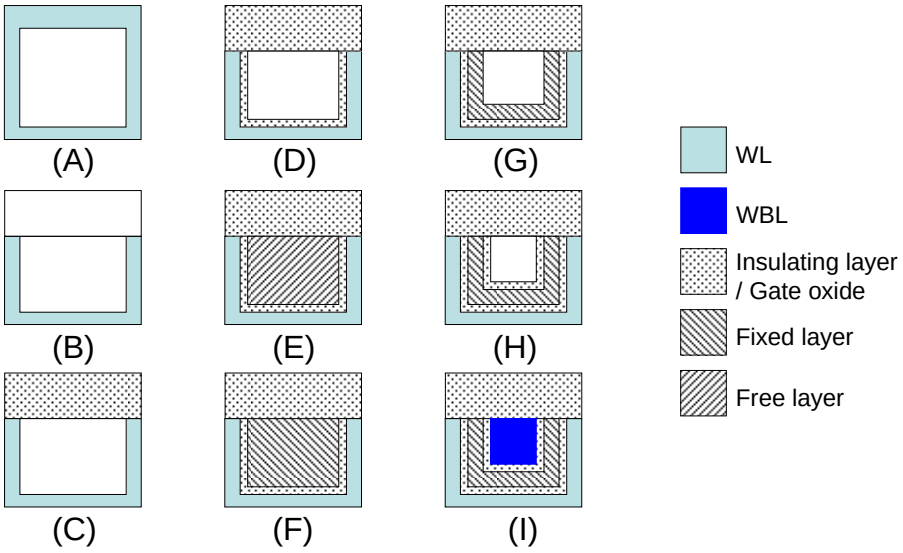

Figure 5: Additional process steps for realizing stacked type NAND MRAM memory cell array with WBL using BiCS structure.

That is, (A)Trench hole formation to the substrate, (B)Trench isolation formation for isolating the adjacent memory cells, (C)Insulating layer formation within the trench isolation, (D)Formation of the gate dielectric within the trench hole, (E)Formation of the free layer within the trench hole, (F)Formation of the fixed layer, (G)Trench hole formation to the free and fixed layer, (H) Formation of the insulating layer within the trench hole, and (I)Fabrication of WBL within the trench hole, should be introduced. For realizing (F) the magnetic impurity should be diffused from insulating layer between WLs to previously formed free layer using thermal treatment. Therefore, for realizing N layers of stacked type NAND MRAM memory cell array with WBL using BiCS structure, 2N+9 process steps are required. This number of 2N is smaller than 9N of stacked horizontal plane structure case. Therefore, the bit cost with BiCS type structure is expected to be reduced compared with that with stacked horizontal plane structure.
The view of stacked type NAND MRAM memory cell array without WBL using BiCS structure is shown in Fig.6. 4 memory cells are connected in series for simplicity. The circuit diagram(Fig.6(A)), top view(Fig.6(B)), and cross-sectional view (Fig.6 (C)) are shown in this figure. The memory cell size is $2F*2.5F=5F^2$. This value is almost the same as that of stacked horizontal plane structure of $4F^2$. This is because only spin transistor must be designed within the same horizontal plane. As shown in Fig.6 a NAND structure is fabricated in a vertical direction to the horizontal plane. For realizing this BiCS structure with N layer, after the

formation N layers of the insulating layer and WLs, 6 additional process steps shown in Fig.7(A) –(F) should be adopted.

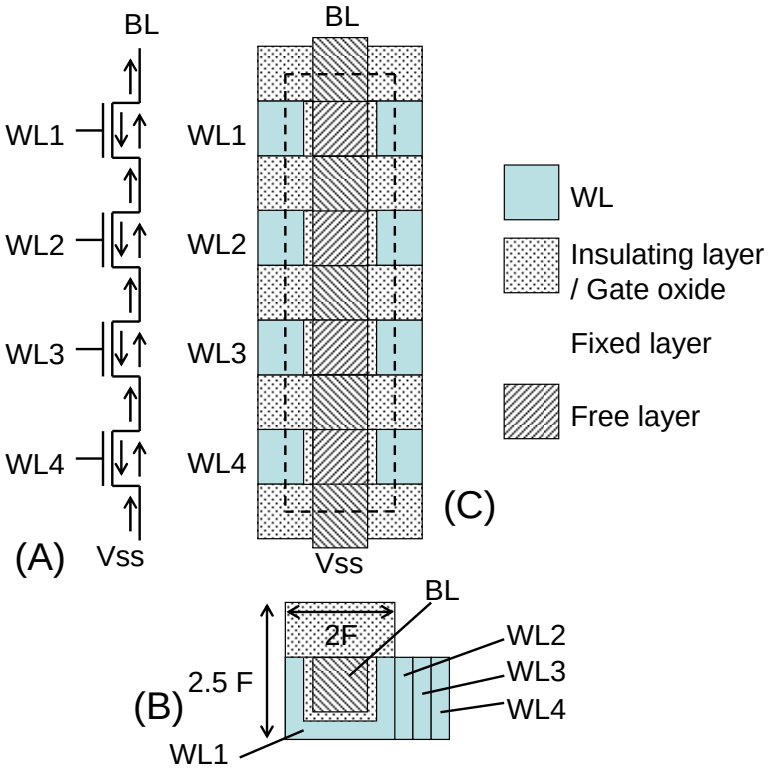

Figure 6: View of stacked type NAND MRAM memory cell array without WBL using BiCS structure, (A)circuit diagram, (B)top view, (C)cross-sectional view.

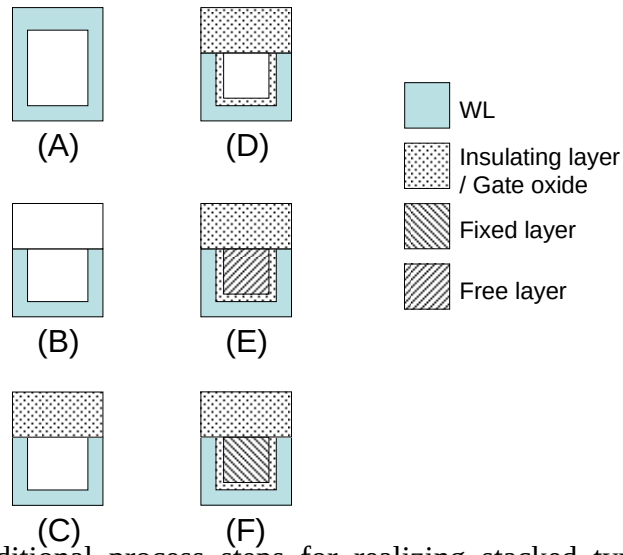

Figure 7: Additional process steps for realizing stacked type NAND MRAM memory cell array without WBL using BiCS structure.

That is, (A)Trench hole formation to the substrate, (B)Trench isolation formation for isolating the adjacent memory cells, (C)Insulating layer formation within the trench isolation, (D)Formation of the gate dielectric within the trench hole, (E)Formation of the free layer within the trench hole, (F)Formation of the fixed layer, should be introduced. This 6 steps is smaller than that with WBL of 9. For realizing N layers of stacked type NAND MRAM memory cell array without WBL using BiCS structure, 2N+6 process steps are required. The number of 2N is smaller than 7N of stacked horizontal plane structure case. Therefore, the bit cost with BiCS type structure is expected to be reduced compared with that with stacked horizontal plane structure.

	NAND flash	**stacked horizontal plane structure (Stacked plane)**	
	Conventional 1 layer type	with WBL	without WBL
Number of layer	1	N	N
Number of process steps	50	50+9N	50+7N
Memory cell array area	$M*4F^2$	$M*4F^2$	$M*4F^2$
Yield	Y	$Y^{(50+9N)/50}$	$Y^{(50+7N)/50}$
Cost of memory cell array	$k*(M*4F^2*50)/Y$	$k*(M*4F^2*(50+9N))/Y^{(50+9N)/50}$	$k*(M*4F^2*(50+7N))/Y^{(50+7N)/50}$
Bit cost	$L*(M*4F^2*50)/(1*Y)$	$L*(M*4F^2*(50+9N))/(N*Y^{(50+9N)/50})$	$L*(M*4F^2*(50+7N))/(N*Y^{(50+7N)/50})$

Figure 8: Estimation of bit cost of memory cell array for stacked type NAND MRAM with stacked plane structure

By using Fig.2 - Fig.7 the bit cost of memory cell array for stacked type NAND MRAM with stacked horizontal plane structure and with BiCS type structure has been compared analytically. And also the bit cost of memory cell array for stacked type NAND MRAM with WBL and without WBL has been compared.

In this analysis the bit cost of NAND flash memory with 1 layer is used as a reference. The bit cost of these structures are estimated by using the formula as shown in Fig.8, 9[7][8]. When the number of the layer is N, the number of residual process steps for realizing stacked type NAND MRAM, such as formation of the peripheral circuit and wiring is assumed to be 50[7][8]. It is assumed that this number of 50 is independent to the memory cell structure. The memory cell area per bit of these structure is $4F^2$ to $9F^2$ (F is feature size). Therefore, using the number of memory cells per one layer, M, memory cell array area of these structures become $M*4F^2$ to $M*9F^2$. The yield of 1 layer NAND flash memory is assumed to be Y. By using the formula Yield(process steps)=$Y^{(\text{number of process steps})/50}$, the yield about process steps of stacked type NAND MRAM can be estimated. And also the yield about pattern area Yield(pattern area)

is estimated using the formula Yield=EXP(-(defect density)*(pattern area)). Yield about pattern area is presented within F(type1) and F(type2) in Fig.9. Cost for memory cell array, fabrication cost for memory cell array, is proportional to memory cell array area and the number of process steps, and inversely proportional to the yield. Therefore, using a constant of proportionality, k, cost of memory cell array of these structures can be estimated (Fig.8,9). Bit cost, cost for one bit, is inversely proportional to number of layer. Therefore, the bit cost can be estimated as shown in Fig.8,9 using a constant of proportionality, L.

	NAND flash	**BiCS structure (BiCS)**	
	Conventional 1 layer type	with WBL	without WBL
Number of layer	1	N	N
Number of process steps	50	50+9+2N	50+6+2N
Memory cell array area	$M*4F^2$	$M*9F^2$	$M*5F^2$
Yield	Y	$F(type1)Y^{(50+9+2N)/50}$	$F(type2)Y^{(50+6+2N)/50}$
Cost of memory cell array	$k*(M*4F^2*50)/Y$	$k*(M*9F^2*(50+9+2N))/(F(type1)/Y^{(50+9+2N)/50}$	$k*(M*5F^2*(50+6+2N))/(F(type2)/Y^{(50+6+2N)/50}$
Bit cost	$L*(M*4F^2*50)/(1*Y)$	$L*(M*9F^2*(50+9+2N))/F(type1)/(N*Y^{(50+9+2N)/50})$	$L*(M*5F^2*(50+6+2N))/F(type2)/(N*Y^{(50+6+2N)/50})$

Figure 9: Estimation of bit cost of memory cell array for stacked type NAND MRAM with BiCS structure

Estimated bit cost of memory cell array for stacked type NAND MRAM vs number of layer is shown in Fig.10-12. The yield of 1 layer NAND flash memory, Y, is used as a parameter (Y=95% for Fig.10, Y=90% for Fig.11, Y=70% for Fig.12). In all cases, at first, the bit cost decreases with increasing the number of layer, and after that increases with increasing the number of layer. This is because, at first, the bit cost decreases with increasing number of layer, and after that the bit cost increases with decreasing yield. This feature is enhanced with decreasing Y. As a result, there is the optimized number of layer where the bit cost of memory cell array becomes minimum value (arrow in Fig.10-12). In Fig.10-12 bit cost of 1 indicates the bit cost of 1 layer NAND flash as a reference. The bit cost of 1 layer NAND flash memory is smallest among the presently available semiconductor memory. In Fig.10-12 optimized number of layer and minimum bit cost are also shown.

For the large value of yield of 95%, the minimum bit cost of BiCS structure becomes smaller than that of stacked plane structure with using larger optimized number of layer (Fig.10).

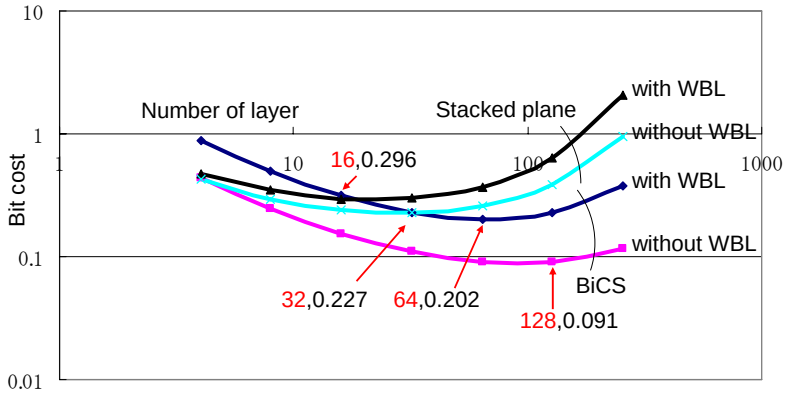

Figure 10: Bit cost of memory cell array for stacked type NAND MRAM vs number of layer. Y=95%.

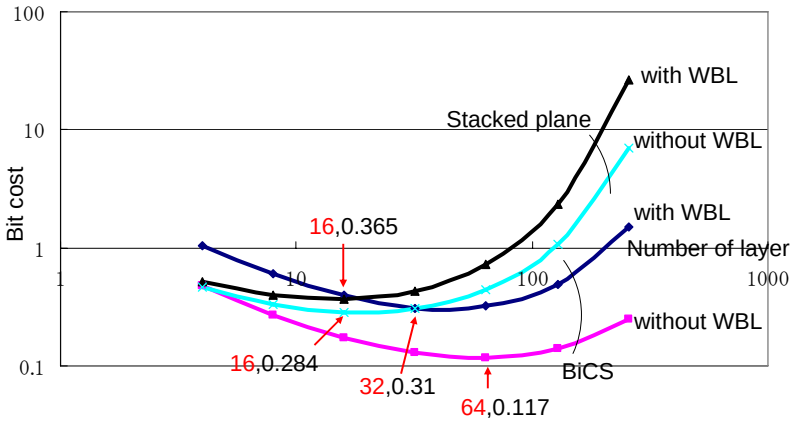

Figure 11: Bit cost of memory cell array for stacked type NAND MRAM vs number of layer. Y=90%.

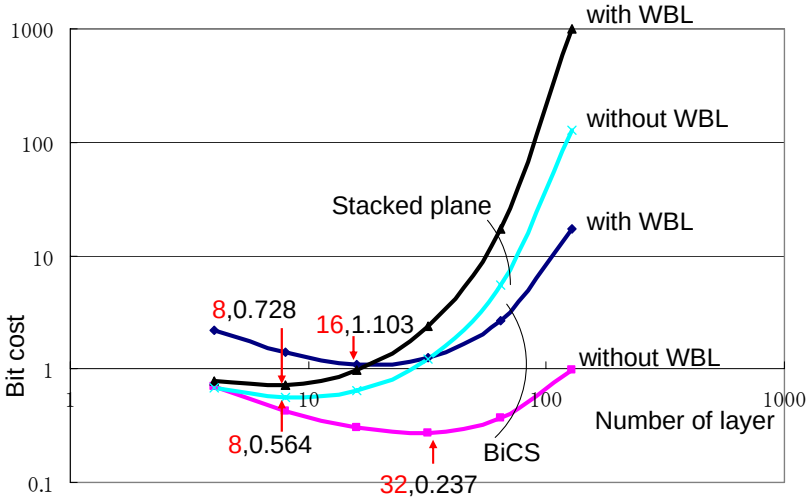

Figure 12: Bit cost of memory cell array for stacked type NAND MRAM vs number of layer. Y=70%.

This is because for BiCS structure by using the large number of layer smaller number of process steps can be realized compared with that with stacked plane structure. For both stacked plane structure and BiCS structure the minimum bit cost for without WBL is smaller than that of with WBL. This is because using without WBL smaller cell size for BiCS structure and smaller number of process steps for stacked plane structure can be realized compared with that with WBL. The bit cost of BiCS type structure is as small as 0.091-0.202 compared with that of 1 layer NAND flash memory using the optimized number of layer of 64-128. This result indicates that because of low bit cost stacked type NAND MRAM with BiCS structure is the promising candidate for replacing the 1 layer NAND flash memory. Of course, the small bit cost of stacked plane structure of 0.227-0.296 is also available for realizing low cost semiconductor memory.
For the smaller value of yield of 70%, the minimum bit cost of BiCS structure without WBL, 0.237, becomes smaller than that of stacked plane structure, 0.564-0.728, with using larger optimized number of layer as the same as Y=95% (Fig.12). However, with WBL case the minimum bit cost of BiCS structure, 1.103, becomes larger than that of stacked plane structure, 0.564-0.728. This is because relative larger memory cell size of $9F^2$ causes larger cost and smaller yield. Therefore, the BiCS structure with WBL is available for larger yield case of 95%.
These results are surmalized in Fig.13.

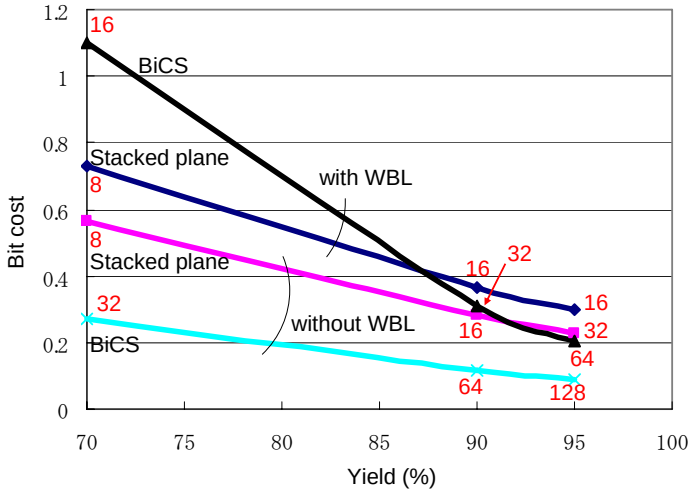

Figure 13: Bit cost of memory cell array for stacked type NAND MRAM vs Y. The optimized number of layer is also indicated.

3 Analysis of bit cost of memory cell array＋Row decoder for stacked type MRAM with NAND structured cell

In section 2 the bit cost of memory cell array has been described. For the case of 1 layered NAND flash memory the bit cost of core circuit, especially for row

decoder can be negligibly small compared with that of memory cell array. However, for the case of stacked type memory with NAND structured cell, the bit cost of row decoder is not be negligibly small. This is because the pattern area of row decoder is proportional to the number of stacked layer. In this section bit cost of memory cell array + row decoder of stacked type NAND MRAM is estimated. The precise circuit and pattern design of row decoder is previously reported for BiCS structure[1][2]. Therefore, the bit cost of memory cell array + row decoder of stacked type NAND MRAM with BiCS structure has been estimated. Fig.14 shows the pattern area of memory cell + row decoder vs number of stacked layer for BiCS structure. In the case that the stacked number is 1, this value becomes reference value of 1. For the case of with WBL, 4K cells are connected to one sided row decoder[1]. For the case of without WBL 8k cells are connected to double ended row decoder[2]. These number of memory cell is determined for realizing the high speed operation competitive DRAM. As shown in this figure when the number of stacked layer is larger than 32, the increase in pattern area of row decoder must be taken into account for the estimation of bit cost.

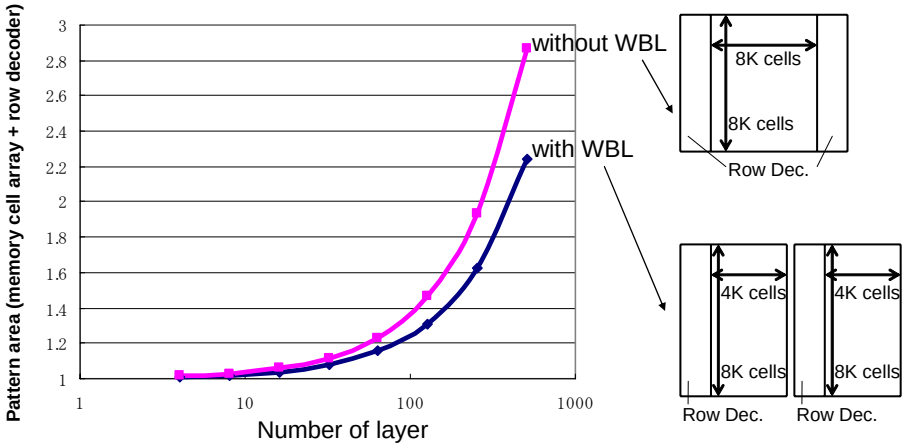

Figure 14: Pattern area of memory cell array + row decoder for stacked type NAND MRAM with BiCS structure vs number of layer.

Bit cost of memory cell array + row decoder for stacked type NAND MRAM with BiCS structure vs number of layer, (Y=90%) is shown in Fig.15. Because of the pattern area increase caused by row decoder the minimum bit cost increased compared with that without row decoder. Furthermore, in the case without WBL the optimum number of layer decreases from 64 to32. For the BiCS structure case small bit cost is achieved with relatively large number of optimized layer. This leads to the relatively large increase of bit cost with row decoder. Therefore, it is very important for BiCS structure case to estimate bit cost with row decoder.

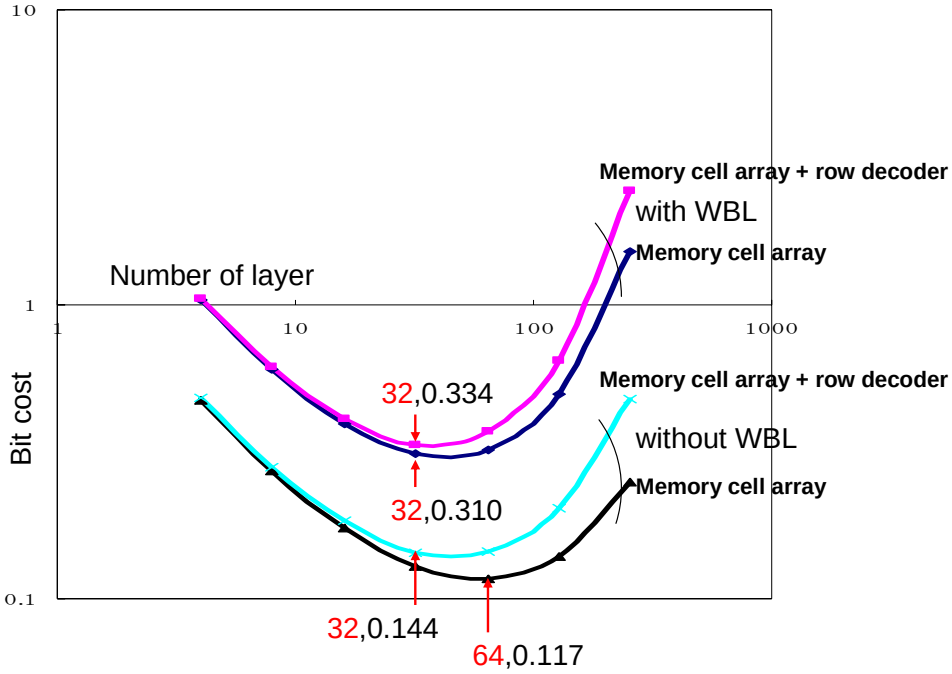

Figure 15: Bit cost of memory cell array + row decoder for stacked type NAND MRAM with BiCS structure vs number of layer. Y=90%.

5 Conclusion

	NAND flash	Stacked plane		BiCS	
	1layer	with WBL	without WBL	with WBL	without WBL
cell size	4F2	4F2	4F2	9F2	5F2
Number of process steps	50	50+9N	50+7N	50+9+2N	50+6+2N
Minimum bit cost	1	0.296	0.227	0.202	0.091
optimized number of layer	——	16	32	64	128

Figure 16: Summary of bit cost of memory cell array. Y=95%.

In this paper the analysis of bit cost of stacked type NAND MRAM has been newly described. Both stacked plane and BiCS architecture is very effective for realizing small bit cost of memory cell array. The reduction rate of bit cost for BiCS is larger with larger yield of Y. The reduction rate of bit cost without WBL is larger than that of WBL. This is because cell size without WBL is smaller than that with WBL for BiCS case, and number of process steps without WBL is

smaller than that with WBL for stacked plane case. These results are summarized in Fig.16. For more accurate estimation of bit cost not only pattern area of memory cell array but also row decoder should be taken into account. Both stacked plane and BiCS architecture is promising candidates for realizing low cost and high speed non-volatile semiconductor memory.

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