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Novel Cell Array Noise Cancelling Design Scheme for Stacked Type MRAM with NAND Structured Cell

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Abstract

In this paper novel cell array noise cancelling design scheme considering memory cell array noise for stacked type NAND MRAM has been newly described. Memory cell array noise which is inherent to stacked type NAND MRAM is newly analyzed. This noise for read operation of 48mV is almost equal to the signal to selected WL of 50mV during read operation. For realizing the cell array noise cancelling the adjacent WLs in the adjacent NAND structure has been successfully used. Circuit design and pattern design of newly proposed row decoder and noise cancelling circuit are described. Using the novel design scheme stable read operation can be achieved with only area penalty of 2.2%. Proposed novel scheme is promising candidates for realizing stable operation of stacked type NAND MRAM.

Keywords: MRAM, NAND structured cell, spin transistor, BiCS, noise

1 Introduction

DRAM is widely used for the main memory of personal computer because of its high speed characteristics. On the other hands, NAND flash memory which has the features of non-volatility and low bit cost is widely used for the storage device of the multi-media data. Universal memory which has both features, DRAM and NAND flash memory, is key technology for the future memory system. Recently, various kinds of stacked type MRAM[1]-[3] and FeRAM[4]-[6] with NAND structured cell have been proposed for the candidate of the universal memory. These memory use one transistor type memory cell, spin transistor[7][8] or FeFET[9][10] connected in series for data storage. These works show that these proposals are promising candidates for realizing high speed competitive to DRAM and low bit cost more than 1 layered NAND flash memory. These works describes the novel read and write scheme which are inherent to stacked type NAND memory and novel design for core circuits such as row decoder. However, the memory cell array noise which is inherent to stacked type NAND memory and design scheme which can cancel this cell array noise has not been reported. Spin transistor for MRAM use the difference of resistance for memory storage. This architecture has the disadvantage about the stable operation compared with that of FeRAM which can use the difference of threshold voltage, VT, for memory storage. In this paper memory cell array noise which is inherent to stacked type NAND MRAM and novel design scheme which can cancel this memory cell array noise have been newly proposed. For realizing this cancelling the adjacent WLs in the adjacent NAND structure has been successfully used.
This paper is organized as follows. Section 2 describes analysis of memory cell array noise during read and write operation which is inherent to stacked type NAND MRAM. Section 3 describes the novel design scheme which can cancel the cell array noise using the adjacent WLs in the adjacent NAND structure. Section 4 describes the circuit design such as row decoder and newly proposed noise cancelling circuit. Finally, conclusion of this work is provided in Section 5.

2 Analysis of memory cell array noise during read and write operation for stacked type NAND MRAM

In this section the analysis of memory cell array noise of stacked type NAND MRAM has been described. For estimating the memory cell array noise, the conventional magnetic writing scheme [1][2] generated by a current flow in perpendicular running write bit line and word line can be adopted (Fig.1). During read operation high voltage of 1V is applied to gate of passed cell transistor. Gate voltage of 0.25V which is by only 0.05V larger than VT (0.2V) is applied to the

selected cell transistor. This small gate voltage is key issue for stable operation of stacked type NAND MRAM. This is because, the resistance of the selected cell should be larger than total resistance of passed memory cell[1][2]. During write operation 2V is applied to selected WL and BL for generating magnetic field.
However, due to the inherent capacitance coupling between the adjacent WLs the cell array noise is generated on the selected WL during read operation as shown in Fig.2. The value of this noise, caused by the capacitance coupling of C_{intra} between the adjacent WLs within the same NAND structure, depends on the position of memory cell within the NAND structure.

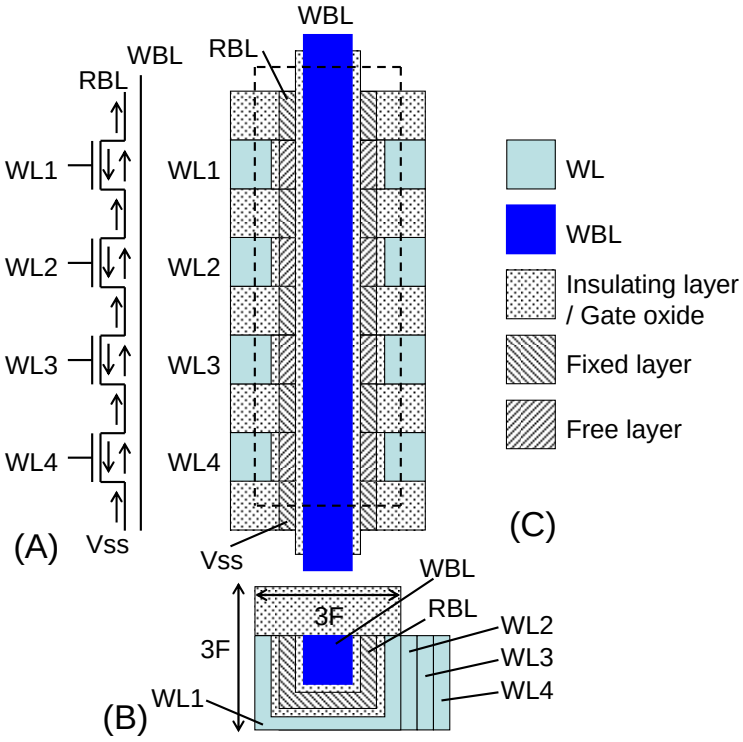

Figure 1: View of stacked type NAND MRAM memory cell array with WBL using BiCS structure, (A)circuit diagram, (B)top view, (C)cross-sectional view.

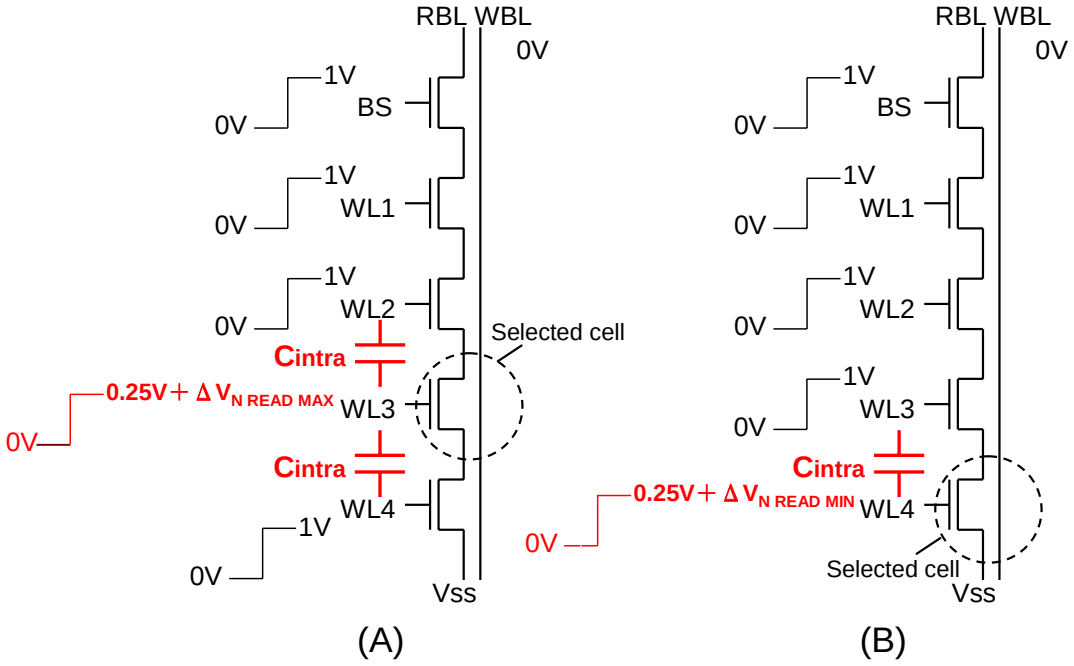

Figure 2: Noise on the selected cell during read operation, (A) maximum noise value case, (B) minimum noise value case.

The maximum cell array noise of $\Delta V_{N\,READ\,MAX}$ is generated for the selected cell, when both side of adjacent passed cells acts as the source of cell array noise (Fig.2 (A)). The minimum cell array noise of $\Delta V_{N\,READ\,MIN}$ is generated for the selected cell, when one side of adjacent passed cell acts as the source of cell array noise (Fig.2 (B)).

The capacitance coupling of C_{intra} between the adjacent WLs within the same NAND structure causes the inherent noise for stacked type NAND MRAM during read operation as shown in Fig.2. Therefore, C_{intra} is estimated using Fig.3 and formula of capacitance which includes fringe effect[11].

The thickness of WL and distance between adjacent WL within the same NAND structure is F[12][13]. F is design rule of 39nm. The distance between adjacent WL of adjacent NAND structure is F. ε_r of dielectric between adjacent WL and gate oxide of memory cell transistor is 3.9 of SiO_2. The channel width of memory cell transistor is 5F. It is assumed that 4K memory cells are connected to one WL. Using C_{intra} and C_{inter} which corresponds to the capacitance coupling between adjacent WLs of adjacent NAND structure the value of cell array noise can be estimated as follows. Cg is gate capacitance of memory cell transistor.

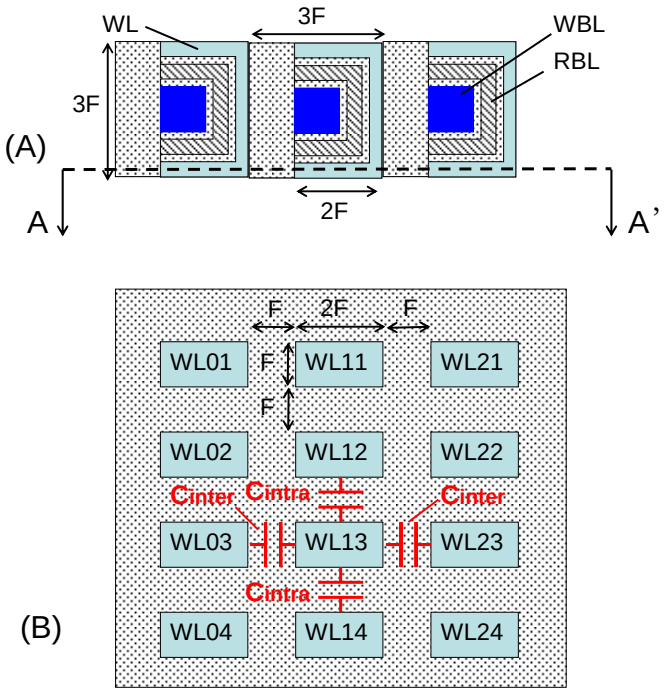

Figure 3: (A)Top view of memory cell array, (B)Cross sectional view of memory cell array of AA' direction of Fig.3(A).

$$\Delta V_{N\,READ\,MAX} = (\,2C_{intra} / (Cg + 2\,C_{intra} + 2\,C_{inter}))*1V \text{ -------- (1)}$$

$$\Delta V_{N\,READ\,MIN} = (\,C_{intra} / (Cg + 2\,C_{intra} + 2\,C_{inter}))*1V \text{ -------- (2)}$$

The estimated value of $\Delta V_{N\,READ\,MAX}$ is 48mV and of $\Delta V_{N\,READ\,MIN}$ is 24mV. The value of 48mV is almost equal to the value of signal voltage on selected WL of 0.25V-0.2V=50mV. This large cell array noise value causes mal-function of memory cell. Therefore, introduction of novel cell array noise cancelling design scheme is the key issue for realizing stable read operation.
During write operation the same value of $\Delta V_{N\,READ\,MAX}$ is generated to the passed WLs. This value is negligibly small compared with the signal of selected WL of 2V. Therefore, extra cancelling scheme is not needed for write operation.

3 Novel cell array noise cancelling design scheme for read operation

In this section the concept of the novel cell array noise canceling design scheme for stacked type NAND MRAM has been newly proposed for read operation. As

described in section 2, the memory cell array noise during read operation, $\Delta V_{N\ READ\ MAX}$, is 48mV. This noise value is very large and almost the same value of signal to selected WL of 50mV. In the novel design scheme it is aimed that large cell array noise of 48mV is cancelled with the proposed technique (Fig.4).

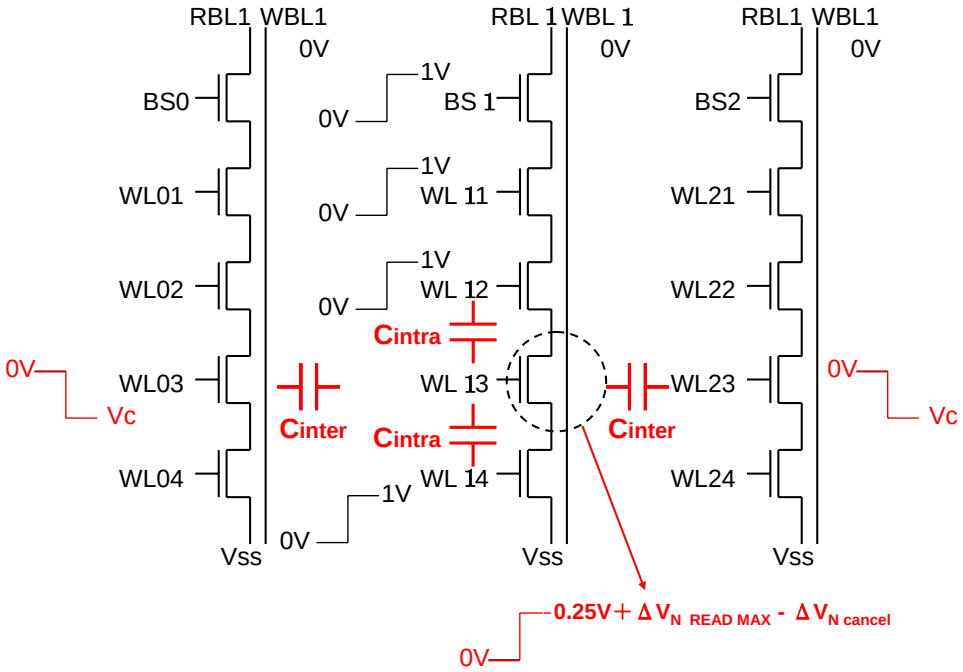

Figure 4: Novel array noise cancelling design during read operation for stacked type NAND DRAM. WL13 is selected.

For canceling the cell array noise the canceling means must be located near the selected WL, WL13 in Fig.4. The adjacent WLs in the adjacent NAND structure, WL03 and WL23, can be used as this noise cancelling means. This noise cancelling technique can be used for only 3D stacked NAND structure. This is because in the case of 2D NAND structure there is no noise cancelling means near the selected WL. When the selected WL, WL13, is activated from 0V to 0.25V, the adjacent WLs, WL03 and WL23, are activated from 0V to negative voltages of V_C. In this time using the capacitance coupling C_{inter} negative noise of $-\Delta V_{N\ CANCEL}$ can be generated. Designing that $\Delta V_{N\ READ\ MAX} = \Delta V_{N\ CANCEL}$, $\Delta V_{N\ READ\ MAX}$ can be successfully cancelled by introducing $\Delta V_{N\ CANCEL}$. For realizing accurate cancelling, V_C must be designed as shown in (3).

$$V_C = -(C_{intra} / C_{inter})*1V \text{ ----------(3)}$$

Using ref[11], (C_{intra} / C_{inter}) can be calculated as follows. (C_{intra} / C_{inter}) =2.21/1.15=1.92. Therefore, for cancelling the memory cell array noise, WL03 and WL23 must be activated from 0V to -1.92V. In Fig.4 it is assumed that

adjacent WLs within the same NAND structure, WL12 and WL14, acts as the passed WLs. If the selected WL, WL14, which is located in the lowest position in the NAND structure as shown in Fig.5, only one side of adjacent WL, WL24, is activated from 0V to -1.92V for canceling the noise of $\Delta V_{N\,READ\,MAX}/2$.

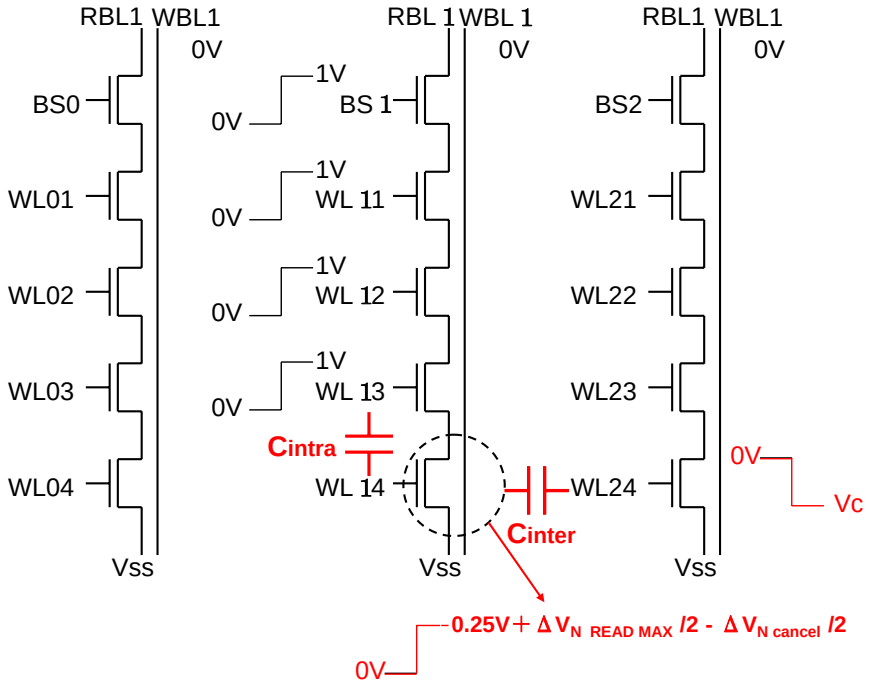

Figure 5: Novel array noise cancelling design during read operation for stacked type NAND DRAM. WL14 is selected.

4 Circuit design of row decoder and newly proposed noise cancelling circuit

For realizing the novel noise cancelling design scheme not only conventional row decoder circuit proposed in ref[2] but also noise cancelling circuit should be newly introduced. The conventional row decoder circuit is shown in Fig.6. Conventional prechage type NOR decoder and WL driver circuit with partial decoded address input is employed. Using this circuit one WL, WL13, is selected for reading the memory cell data. These circuits are placed on the left side of memory cell array. In the right side of memory cell array circuit about write operation is placed. In this row decoder circuit 4 stages of NAND structure and 4 input of NOR decoder is assumed for simplicity. In order to reduce the noise on

the unselected WLs for unselected NAND structure, noise killer transistor, its gate is connected to invert signal of output for NOR, BS7, is connected to WLs. If this circuit is employed to the newly proposed scheme noise cancelling signal on WLs, WL03 and WL23, is destroyed by this noise killer transistor. Furthermore, adjacent NAND structures, with which belongs to WL03 and WL23, can not be activated with the conventional NOR decoder placed on the left side of memory cell array.

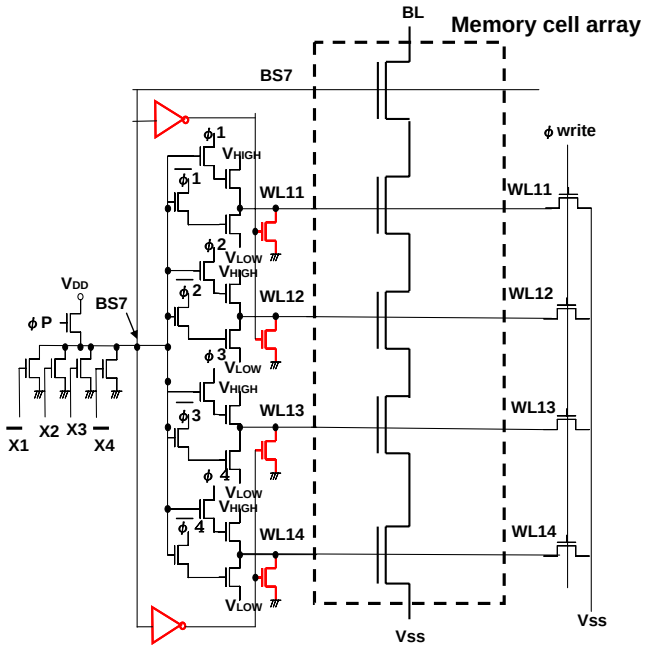

Figure 6: Conventional row decoder circuit in ref[2].

In order to overcome this problem row decoder and noise cancelling circuit are newly proposed, (Fig.7). It is assumed that WL13 which belongs to 7th NAND structure is selected. Therefore, WL03 of adjacent 6th NAND structure and WL23 of adjacent 8th NAND structure must be activated for noise cancelling means. In this figure not only circuit about 7th NAND structure but also circuit of quasi NOR decoder for 6th and 8th NAND structure are shown. Addition to the NOR decoder of left side of memory cell array for selecting the WL13, quasi NOR decoder is newly introduced for selecting the noise cancelling means, WL03 and WL23, on the right side of memory cell array. The output of this quasi NOR decoder, BS6R, BS7R and BS8R, are used as follows. 2 input NOR circuit, its inputs are BS6R and BS8R is used for activating 7th NAND structure for noise cancelling. When 6th or 8th NAND structure is selected this 7th NAND structure is activated for noise cancelling. 3 input NOR circuit, its inputs are BS6R, BS7R and BS8R is used for disabling the noise killer transistor which is connected left edge

of WLs. If 7th NAND structure is selected not only noise killer transistor for 7th NAND structure but also transistors for 6th and 8th NAND structure can be disabled using this circuit. In the conventional circuit of ref[2] the write circuit which connect right edge of WL to Vss is formed with only one transistor. In the newly proposed scheme this circuit is consisted with 2 transistor connected in series. Using this circuit only WL03 and WL23 can be connected to negative voltage of Vc for read operation and only left edge of selected WL, WL13, can be connected to Vss for write operation. For generating Vss during write operation and Vc during read operation signal of Vc/Vss is generated with row decoder and noise cancelling

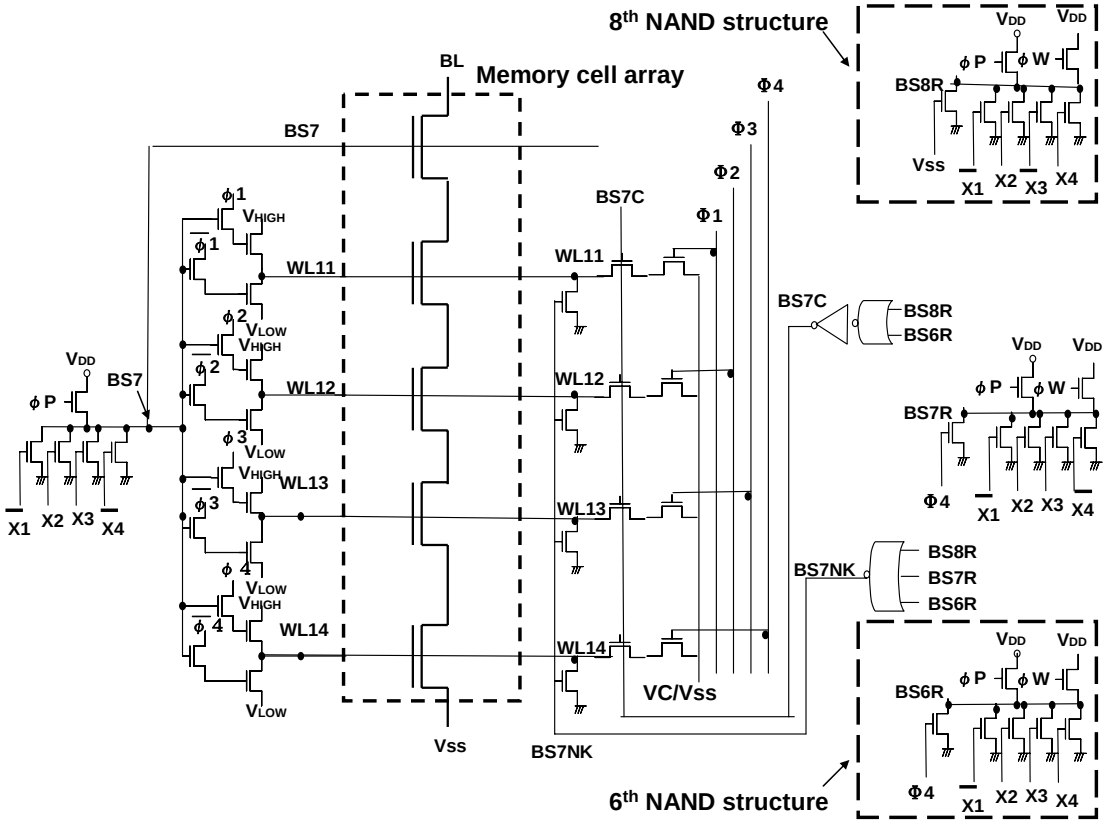

Figure 7: Newly proposed row decoder circuit and noise cancelling circuit.

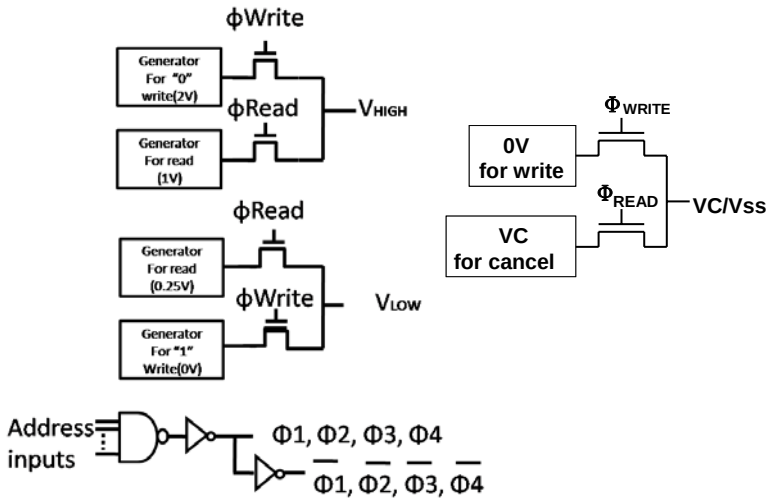

Figure 8: Newly proposed row decoder and noise cancelling drive circuit.

drive circuit, (Fig.8). Using these circuit newly proposed noise cancelling scheme can be realized. The timing of read operation of newly proposed method is shown in Fig.9.

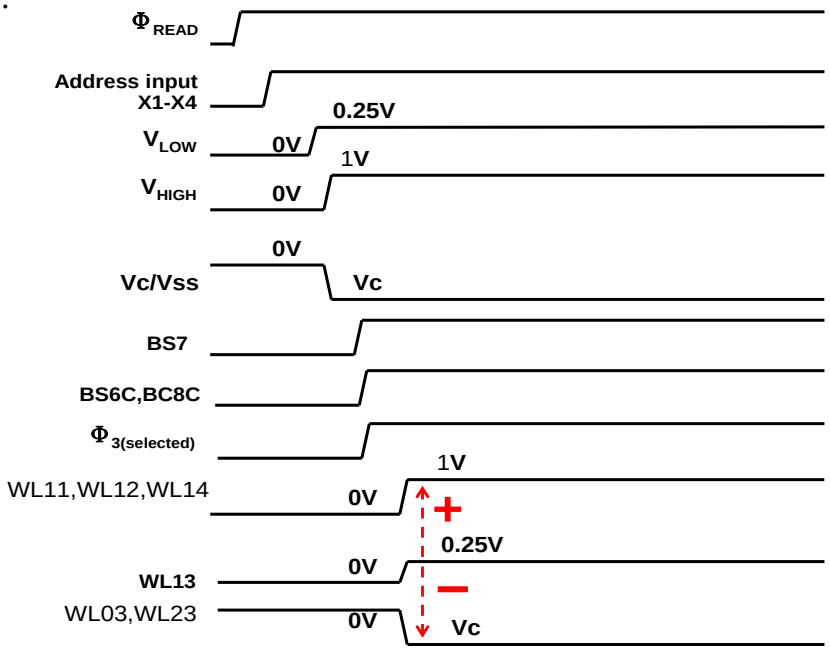

Figure 9: Timing of read operation of newly proposed scheme.

Corresponding circuits are summalized in Fig.10. In this figure it is assumed that WL13 of 7th NAND structure is selected and that WL03 of adjacent 6th NAND structure and WL23 of adjacent 8th NAND structure are activated as the noise cancelling means. If WL14, lowest stage of 7th NAND structure is selected only

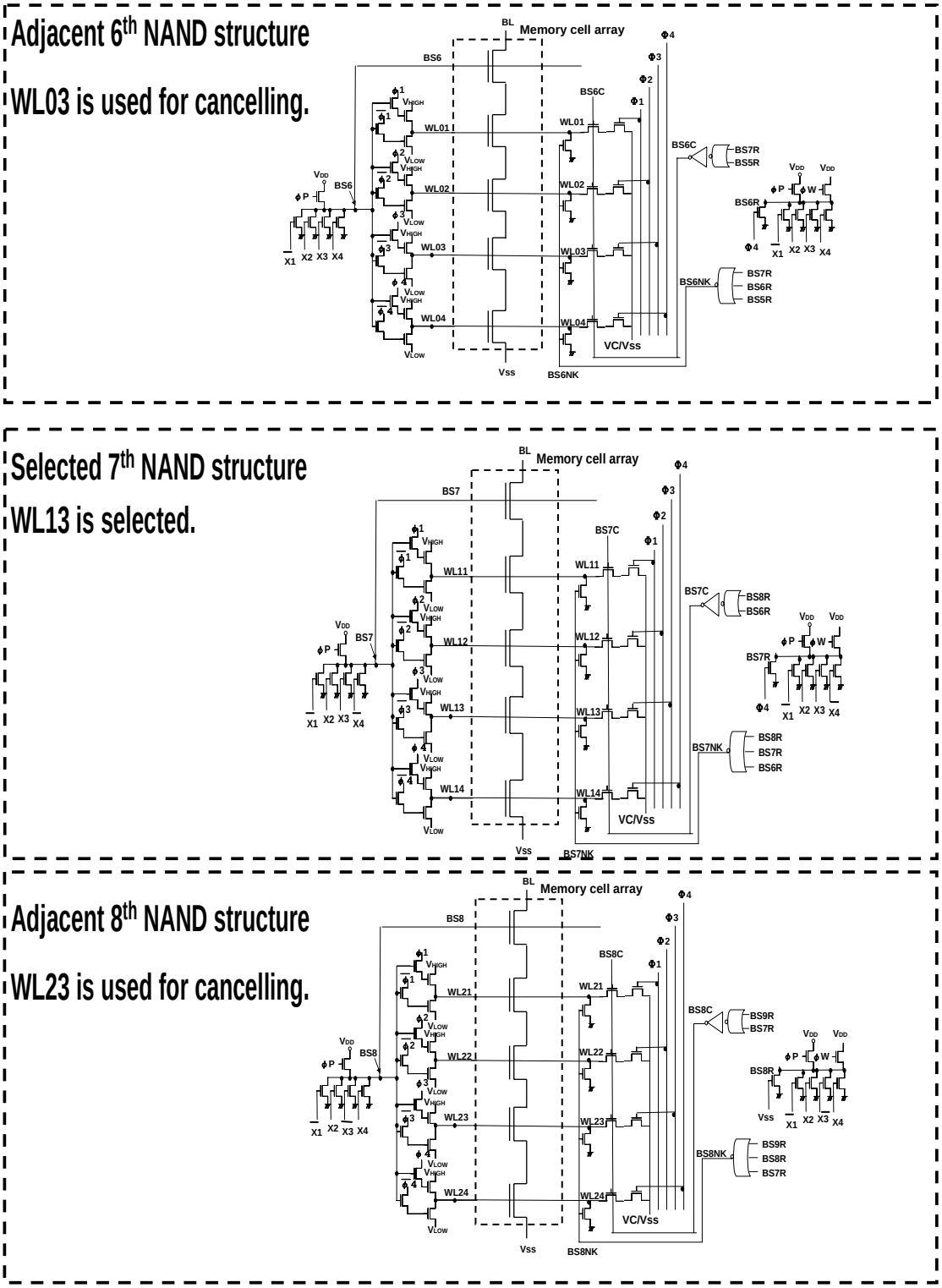

Figure 10: Row decoder and noise cancelling circuit corresponding to 6th, 7th and 8th NAND structure.

WL24 of 8th NAND structure is activated as noise canceling means. In this time WL04 of 6th is not activated. This procedure can be achieved by changing the input of quasi NOR gate of noise cancelling circuit ϕ4 or VSS as shown in Fig.7 and Fig.10.
With introducing the novel noise cancelling circuit, the pattern area of row decoder + noise canceling circuit increased compared with that of conventional scheme[2].
The pattern area is estimated using the following assumptions. 13 address signal are inputed into NOR decoder. This corresponds to 8K NAND structure. That is, 8K memory cells are connected to one BL. 64 of stacked layer is employed for reducing the bit cost. 4K memory cells are connected to one WL. Therefore, one memory cell array realizes 4K*8K*64=2Gbit stacked NAND MRAM. The key pattern design for estimating the pattern area is newly proposed noise cannelling circuit located in the right side of memory cell area. The pattern of noise cancelling circuit is shown in Fig.11. Using SGT[2][15][16] and 2 layer of wiring, upper metal wiring and lower metal wiring, complex pattern of noise cannelling circuit can be successfully designed within the small pattern area of 15F*3F.

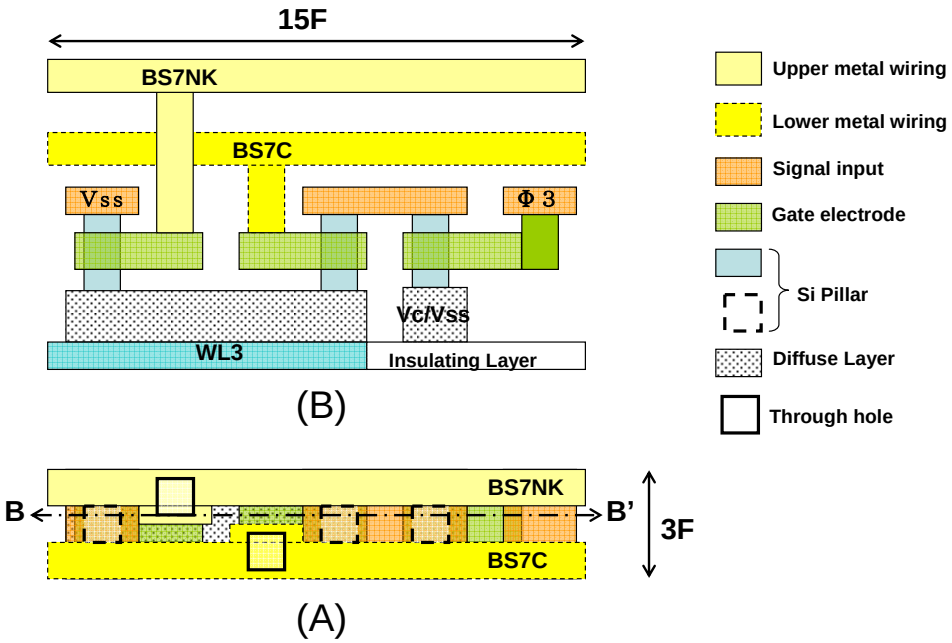

Figure 11: Pattern design of newly proposed noise cancelling circuit. (A)Top view, (B)Cross sectional view of BB'.

Using this pattern design pattern area penalty of this scheme can be reduced to only 2.2% without performance penalty. The estimated results are summalized in Fig.12. With only 2.2% of pattern increase stable operation for read period can be achieved. Newly proposed scheme is the promising candidate for realizing future stacked type NAND MRAM with stable read operation.

	Conventional scheme	Proposed novel design scheme
	ε F=3.9	ε F=3.9
ΔVN READ MAX − ΔVN CANCEL	48mV	0mV
Distance between WLs	F	F
Bit cost	1	1.022
additional delay time	0ns	0ns
New process/ circuit technology	———	Additional circuit to row decoders
Read operation	Mal-function	Stable operation

Figure 12: Summary of the newly proposed novel design scheme.

For realizing the proposed novel design scheme accurate estimation of Vc described in (3) is very important. (C_{intra} / C_{inter}) of (3) is fluctuated from the designed value of 1.92 due to variation of thickness of WL and distance between adjacent WLs. Therefore, for realizing the accurate estimation of Vc die-to-die monitoring using fuse device[17][18] should be introduced. With device scaling the value of (C_{intra} / C_{inter}) of 1.92 and the voltage of passed WL of 1V will be chanced from the designed value. In this case proposed noise cancelling scheme can be realized with calibration of voltage of Vc. The newly proposed scheme has much tolerance for variation of device parameter and device scaling.

5 Conclusion

In this paper novel cell array noise cancelling design scheme considering memory cell array noise for stacked type NAND MRAM has been newly described. Memory cell array noise which is inherent to stacked type NAND MRAM is newly analyzed. This noise for read operation of 48mV is almost equal to the signal to selected WL of 50mV during read operation. For realizing the cell array noise cancelling the adjacent WLs in the adjacent NAND structure has been successfully used. Circuit design and pattern design of newly proposed row decoder and noise cancelling circuit are described. Using the novel design scheme stable read operation can be achieved with only area penalty of 2.2%. Proposed novel scheme is promising candidates for realizing stable operation of stacked type NAND MRAM.

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