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Design Scheme Considering Memory Cell Array Noise for Stacked Type MRAM with NAND Structured Cell

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Abstract

In this paper design scheme considering memory cell array noise for stacked type NAND MRAM has been newly described. Memory cell array noise which is inherent to stacked type NAND MRAM is newly analyzed. This noise for read operation of 48mV is almost equal to the signal to selected WL of 50mV during read operation. 3 kinds of design method, the increase in distance between adjacent WLs, introduction of high-k insulating layer, and air gap, which can reduce the memory cell array noise has been newly proposed. Furthermore, the novel design method which uses the memory cell array noise caused by the conventional scheme for generating the signal of 50mV has been newly proposed. These proposed schemes are promising candidates for realizing stable operation of stacked type NAND MRAM.

Keywords: MRAM, NAND structured cell, spin transistor, BiCS, noise

1 Introduction

DRAM is widely used for the main memory of personal computer because of its high speed characteristics. On the other hands, NAND flash memory which has the features of non-volatility and low bit cost is widely used for the storage device of the multi-media data. Universal memory which has both features, DRAM and NAND flash memory, is key technology for the future memory system. Recently, various kinds of stacked type MRAM[1]-[3] and FeRAM[4]-[6] with NAND structured cell have been proposed for the candidate of the universal memory. These memory use one transistor type memory cell, spin transistor[7][8] or FeFET[9][10] connected in series for data storage. These works show that these proposals are promising candidates for realizing high speed competitive to DRAM and low bit cost more than 1 layered NAND flash memory. These works describes the novel read and write scheme which are inherent to stacked type NAND memory and novel design for core circuits such as row decoder. However, the memory cell array noise which is inherent to stacked type NAND memory and design method which takes into account this memory cell array noise has not been reported. Spin transistor for MRAM use the difference of resistance for memory storage. This architecture has the disadvantage concerning the stable operation compared with that of FeRAM which can use the difference of threshold voltage, VT, for memory storage. In this paper memory cell array noise which is inherent to stacked type NAND MRAM and novel design method which takes into account this memory cell array noise has been newly proposed.
This paper is organized as follows. Section 2 describes the analysis of memory cell array noise during read and write operation which is inherent to stacked type NAND MRAM. Section 3 presents 3 kinds of design method which can reduce the memory cell array noise described in section 2. Section 4 describes the novel design scheme which uses the memory cell array noise for generating the signal for read operation. Finally, a conclusion of this work is provided in Section 5.

2 Analysis of memory cell array noise during read and write operation for stacked type NAND MRAM

In this section the analysis of memory cell array noise of stacked type NAND MRAM has been described. For estimating the memory cell array noise, the conventional magnetic writing scheme [1][2] generated by a current flow in perpendicular running write bit line and word line is adopted (Fig.1). During read operation high voltage of 1V is applied to gate of passed cell transistor. Gate voltage of 0.25V which is by only 0.05V larger than VT (0.2V) is applied to the selected cell transistor. This small gate voltage is key issue for stable operation of

stacked type NAND MRAM. This is because, the resistance of the selected cell should be larger than total resistance of passed memory cell[1][2]. During write operation 2V is applied to selected WL and BL for generating magnetic field.
However, due to the inherent capacitance coupling between the adjacent WLs the cell array noise is generated on the selected WL during read operation as shown in Fig.2. The value of this noise, caused by the capacitance coupling of C_{intra} between the adjacent WLs within the same NAND structure, depends on the position of memory cell within the NAND structure.

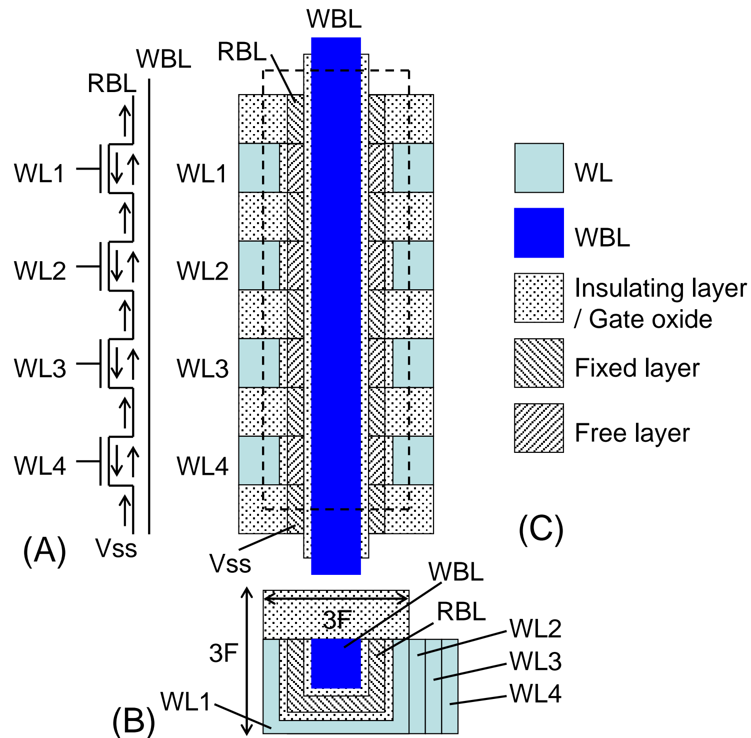

Figure 1: View of stacked type NAND MRAM memory cell array with WBL using BiCS structure, (A)circuit diagram, (B)top view, (C)cross-sectional view.

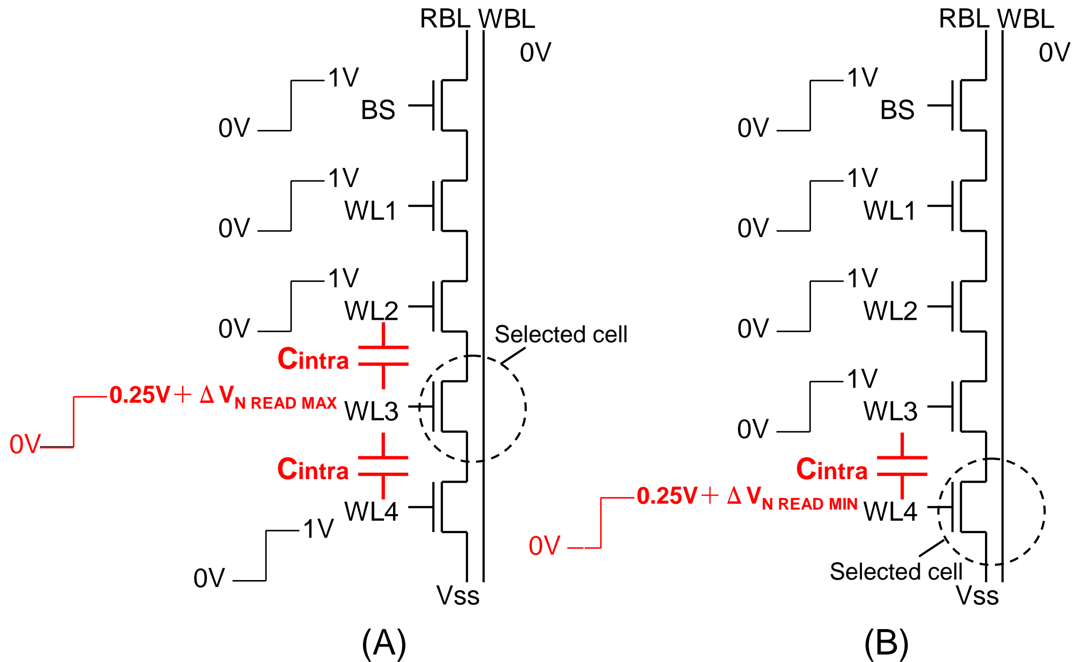

Figure 2: Noise on the selected cell during read operation, (A) maximum noise value case, (B) minimum noise value case.

The maximum cell array noise of $\Delta V_{N\ READ\ MAX}$ is generated for the selected cell which both side of adjacent passed cells acts as the source of cell array noise (Fig.2 (A)). The minimum cell array noise of $\Delta V_{N\ READ\ MIN}$ is generated for the selected cell which one side of adjacent passed cell acts as the source of cell array noise (Fig.2 (B)). This capacitance coupling of C_{intra} between the adjacent WLs within the same NAND structure causes the noise on the passed transistor which is adjacent to selected cell during write operation as shown in Fig.3. The value of cell array noise is $\Delta V_{N\ READ\ MIN} *(2V/1V)= \Delta V_{N\ READ\ MAX}$.

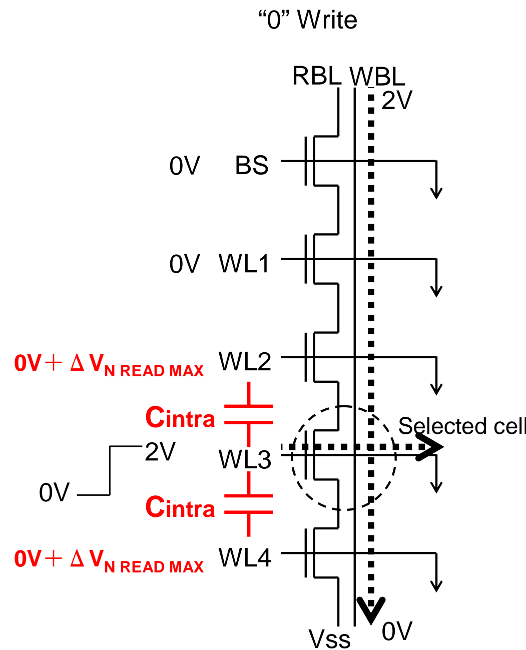

Figure 3: Noise on the passed cells which is generated from the adjacent selected cell during write operation.

The capacitance coupling of C_{intra} between the adjacent WLs within the same NAND structure causes the inherent noise for stacked type NAND MRAM during read and write operation as shown in Fig.2 and Fig.3. Therefore, C_{intra} is estimated using Fig.4 and formula of capacitance which includes fringe effect[11].
The thickness of WL and distance between adjacent WL within the same NAND structure is F[12][13]. F is design rule of 39nm. The distance between adjacent WLs of adjacent NAND structure is F. ε r of dielectric between adjacent WL and gate oxide of memory cell transistor is 3.9 of SiO_2. The channel width of memory cell transistor is 5F. It is assumed that 4K memory cells are connected to one WL. Using C_{intra} and C_{inter} which corresponds to the capacitance coupling between adjacent WLs of adjacent NAND structure the value of cell array noise can be estimated using (1),(2). Cg is gate capacitance of memory cell transistor.

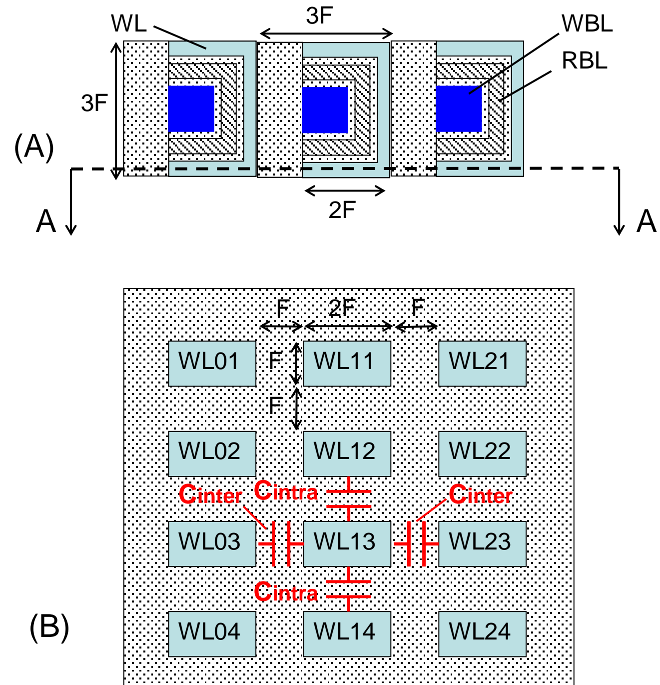

Figure 4: (A)Top view of memory cell array, (B)Cross sectional view of memory cell array of AA' direction of Fig.4(A).

$$\Delta V_{N\ READ\ MAX} = (2C_{intra} / (Cg + 2\ C_{intra} + 2\ C_{inter})) * 1V \quad \text{-------- (1)}$$

$$\Delta V_{N\ READ\ MIN} = (C_{intra} / (Cg + 2\ C_{intra} + 2\ C_{inter})) * 1V \quad \text{-------- (2)}$$

The estimated value of $\Delta V_{N\ READ\ MAX}$ is 48mV and of $\Delta V_{N\ READ\ MIN}$ is 24mV. The value of 48mV is almost equal to the value of signal voltage on selected WL of 0.25V-0.2V=50mV. This large cell array noise value causes mal-function of memory cell. Therefore, the reduction of this large noise and the introduction of novel circuit scheme which takes into account this large noise are key issue for realizing stable read operation.

During write operation this large value of $\Delta V_{N\ READ\ MAX}$ is generated. However, the signal value of selected WL during write operation is as large as 2V. Compared with this large signal of 2V, the value of noise of 48mV is negligibly small. The extra technology for write operation is not needed. Therefore, the reduction of this large memory cell array noise and the introduction of novel design scheme which takes into account this large noise is considered for read operation in the next chapter.

3 Reduction of memory cell array noise during read operation for stacked type NAND MRAM

For reducing memory cell array noise of 48mV 3 kinds of scheme have been described in this chapter.

First is enlargement of the distance between adjacent memory cells within the same NAND structure. The cell array noise between adjacent memory cell can be reduced inversely proportional to the distance. The enlargement of the distance can be achieved with increasing the thickness of dielectric layer between WLs (Fig.1). If the NAND structure is formed within the X-Y plane as the conventional 2 dimensional LSI, this enlargement results in the increase in memory cell area. On the other hand this enlargement can be realized without sacrificing memory cell area for the stacked type NAND MRAM. Furthermore, this scheme can be realized without extra new process technology.

Second is reduction of ε r of insulator layer from 3.9 of SiO_2 to 2. The insulator layer with ε r of 2 is used for presently available CMOS LSI[14]. With minor improvement of these technology insulator layer of ε r of 2 will be introduced to stacked type NAND MRAM. Not only for insulator layer between WLs within the same NAND structure but also for isolation between adjacent NAND structure this technology can be used. As a result, not only C_{intra} but also C_{inter} can be reduced.

Third is introduction of air gap for reducing the ε r from 3.9 to 1[15][16]. Not only for isolation layer between WLs within the same NAND structure but also for isolation between adjacent NAND structure this technology will be used. As a result, both C_{intra} and C_{inter} can be drastically reduced to 1/3.9=26%. For introducing the air gap technology within the stacked type NAND MRAM, process steps for formation of spin transistor must be drastically changed as shown in Fig.5. For the case of conventional technology after the formation of N layers of WLs and insulating layers trench hole is fabricated (Fig.5 (A), top

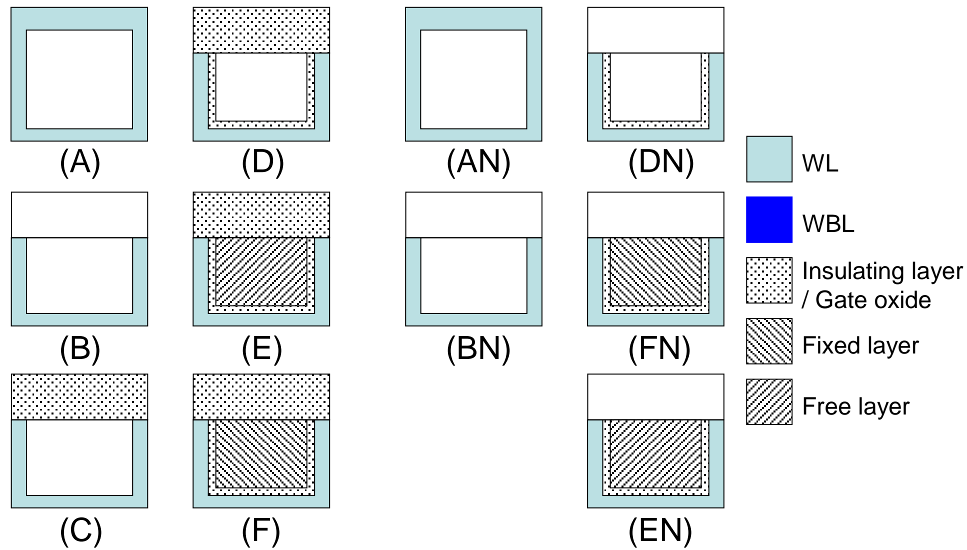

Figure 5: Process flows for formation of spin transistor. (A)-(F) correspond to conventional case of ε r=3.9. (AN)-(EN) correspond to air gap technology case.

view). After that trench isolation between adjacent NAND structure is formed (Fig.5(B)). Then within this trench isolation insulating layer is formed (Fig.5(C)). After formation of gate oxide within trench hole (Fig.5(D)), free layer of spin transistor is fabricated within trench hole (Fig.5(E)). Finally, fixed layer of source/drain is fabricated (Fig.5(F)). For realizing fixed layer of source/drain magnetic material within the isolation layer is diffused into the previously formed free layer with the thermal treatment. For the air gap technology case Fig.5(C) is not needed. And also the process sequence from Fig.5(E) to Fig.5(F) is changed from Fig.5(FN) to Fig.5(EN). Furthermore, for formation of free layer magnetic material within WL is diffused into the previously formed fixed layer through the gate dielectric with the thermal treatment.

The first method can be easily combined to second and third method.

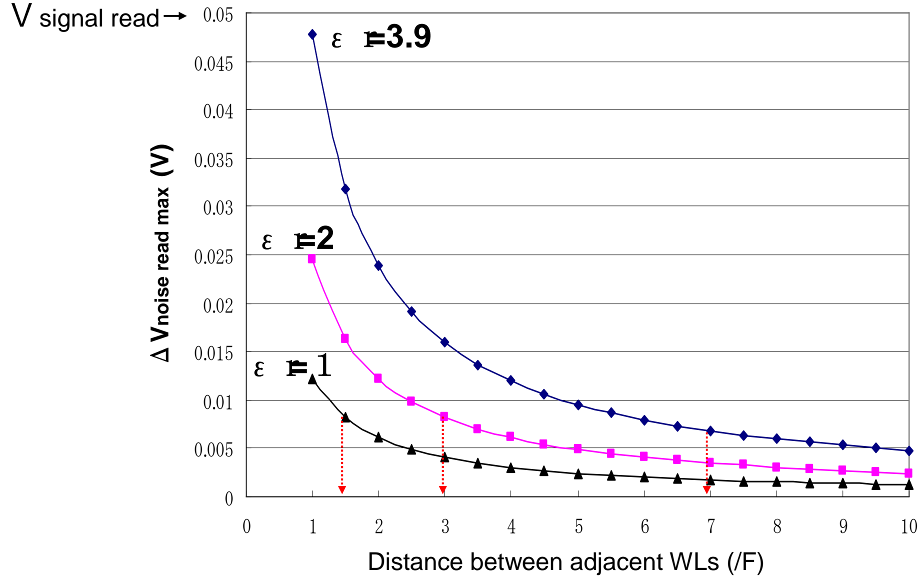

Figure 6: $\Delta V_{N\ READ\ MAX}$ vs distance between adjacent WLs for various value of ε r.

Estimated $\Delta V_{N\ READ\ MAX}$ vs distance between adjacent WLs for various value of ε r =1, 2, 3.9 is shown in Fig.6. For realizing the stable operation $\Delta V_{N\ READ\ MAX}$ must be reduced to less than 20% of read signal of 50mV. It is 10mV. For realizing $\Delta V_{N\ READ\ MAX}$ of 10mV, the distance between adjacent WLs must be enlarged from F to 7F for ε r=3.9, to 3F for ε r =2, to 1.5F for ε r =1 case.

For the conventional case (ε r=3.9) 1 layer of memory cell can be stacked with trench depth of F+F=2F as shown in Fig.4. For this case large $\Delta V_{N\ READ\ MAX}$ of 48mV leads to the mal-function. If the distance between adjacent WL is enlarged from F to 7F the stable operation can be achieved. This leads to the F+7F=8F trench depth for one layer. This increase in trench depth from 2F to 8F will reduce the number of layer. This is because maximum aspect ratio of trench, (trench depth)/(diameter of trench of F) is limited to 150-200 for the process repeatability. Maximum trench depth of 200F leads to the maximum number of layer of 200F/8F=25. As a result, maximum number of layer is limited to 16 of 2^4.

For the case of ε r =2 the same kind of upper limitation of number of layer must be considered as follows. When the distance between adjacent WL is enlarged from F to 3F the stable operation can be achieved. This leads to the F+3F=4F trench depth for one layer. This increase in trench depth from 2F to 4F will reduce the number of layer. Maximum trench depth of 200F leads to the maximum number of layer of 200F/4F=50. As a result, maximum number of layer is limited to 32 of 2^5.

For the case of ε r =1 upper limitation of number of layer is almost the same as the conventional case as follows. When the distance between adjacent WL is enlarged from F to 1.5F the stable operation can be achieved. This leads to the F+1.5F=2.5F trench depth for one layer. This increase in trench depth from 2F to 2.5F will not reduce the number of layer. Maximum trench depth of 200F leads to the maximum number of layer of 200F/2.5F=80. As a result, maximum number of layer is limited to 64 of 2^6. This layer number of 64 is the same as the optimum number of layer for realizing minimum bit cost for the conventional scheme[17].
From the above analysis it is found that if $\Delta V_{N\ READ\ MAX}$ should be reduced to 10mV, the maximum number of layer must be limited to 16 for ε r =3.9 case and to 32 for ε r =2 case and to 64 for ε r =1 case. These limitation results in the increase of minimum bit cost compared with that previously report in ref[17]. These limitation is shown in Fig.7 with the relationship between bit cost and number of layer of ref[17].

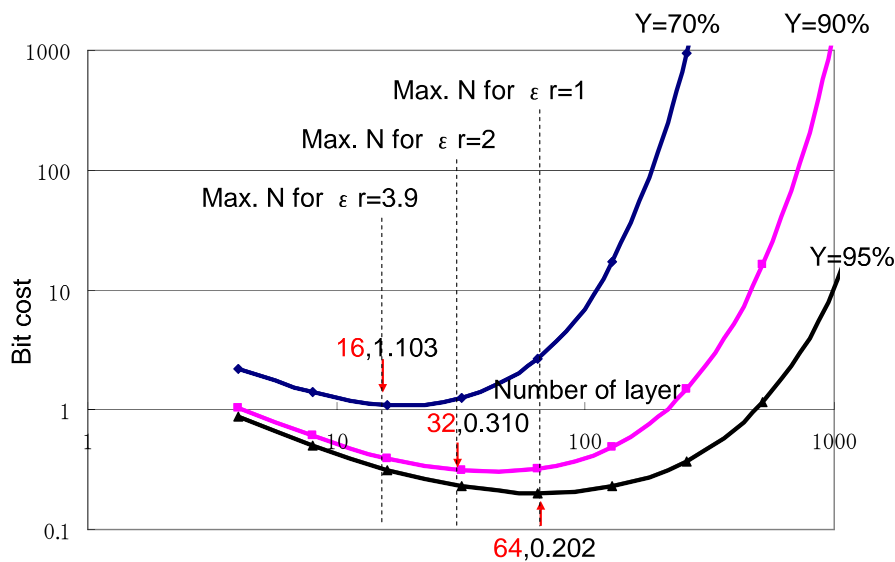

Figure 7: Bit cost vs number of layer for Stacked NAND MRAM[17] with upper limitation of stacked layer of N for stable operation.

Y is yield of 1 layered NAND flash memory. The number of layer and minimum bit cost are also shown in the figure. For Y=95% case the bit cost becomes 1.56 times larger than the minimum value of 0.202 for ε r =3.9 case and 1.14 times larger than 0.202 for ε r =2 case. For Y=90% case the bit cost becomes 1.27 times larger than the minimum value of 0.202 for ε r =3.9 case. On the other hand for ε r =1 case minimum bit cost can be achieved without sacrificing the stable operation. These results are summarized in Fig.8.

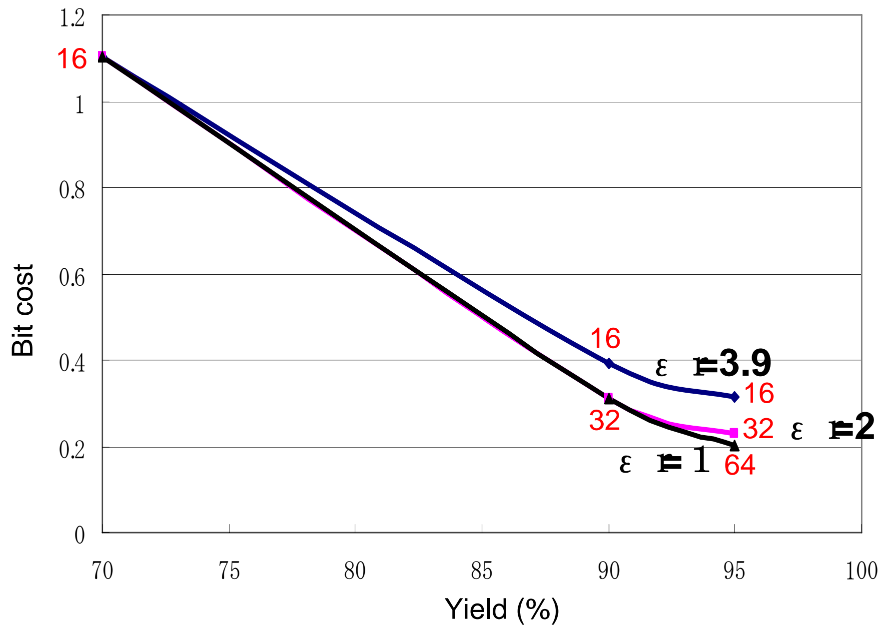

Figure 8: The obtained minimum bit cost vs Y with parameter of ε r for stable operation. The number of layer is also indicated.

As shown in Fig.7,8 the minimum bit cost increases compared with that of conventional case for ε r =2 and ε r =3.9 case. This is because for stable operation distance between WLs must be increased compared with F for conventional scheme. This increase results in the increase of BL delay time. This is because capacitance of bit line per memory cell is proportional to the distance between WLs. Therefore, BL delay time which is proportional to capacitance of BL per memory cell increases with increasing in the distance between WLs. The delay time of BL is summarized in Fig.9. The obtained BL delay time for ε r =1 and ε r =2 case is small enough for realizing high speed characteristics competitive to DRAM. However, the BL delay time for ε r =3.9 is large value of 9.03ns. Because of this large value high speed characteristics competitive to DRAM becomes difficult.

As shown in Fig.9 newly proposed first scheme of ε r =3.9 have the drawback of large bit cost and large BL delay time. On the other hand newly proposed third scheme of ε r =1 requires the new process technology of the air gap process and the diffusion of magnetic material from WL. The newly proposed second scheme of ε r =2 realizes relatively low bit cost and small BL delay time compared with that with ε r =3.9 case using relatively realistic high-k process compared with that with ε r =1 case.

	Conventional scheme	Newly proposed 3kinds of noise reduction scheme		
	ε_r=3.9	ε_r=3.9	ε_r=2	ε_r=1
ΔVN READ MAX	48mV	Less than 10mV	Less than 10mV	Less than 10mV
Distance between WLs	F	7F	3F	1.5F
Bit cost	1	1.27-1.56	1.14	1
BL delay time	1.29ns	9.03ns	3.87ns	1.94ns
New process technology	——	——	Process for Low k	Air gap process Diffusion from WL

Figure 9: Summary of newly proposed 3 kinds of noise reduction scheme with the conventional scheme as a reference.

4 Novel design scheme which uses the memory cell array noise for generating the signal for read operation

In section 3, 3 kinds of memory cell array noise reduction scheme during read operation for stacked type NAND MRAM has been described. These methods focused to reduce the cell array noise for realizing stable operation during read operation. In this section the novel design scheme which uses the memory cell array noise caused by the conventional scheme for generating the signal for read operation. As described in section 2, the memory cell array noise during read operation, $\Delta V_{N\ READ\ MAX}$, is 48mV. This noise value is very large and almost the same value of signal to selected WL of 50mV. The novel design scheme focuses the fact that $\Delta V_{N\ READ\ MAX}$ is almost the same value as signal voltage of 50mV. If the selected WL is precharged to threshold voltage of 0.2V, the selected WL can be automatically charged to 0.25V using the capacitance coupling between selected WL and adjacent passed WLs when the passed WL is charged from 0V to1V (Fig.10). This design scheme assisted by memory cell array noise can be realized without reduction of the memory cell array noise described in section 3. For using the memory cell array noise as the signal generating tool, the value of memory cell array noise must be independent to the location of selected WL. However, the value of memory cell array noise with conventional scheme depends to the location as shown in Fig.2. In order to overcome this problem transistor, gate signal of BS is connected in the lowest stage of NAND structure, is newly introduced for the novel design scheme as shown in Fig.10.

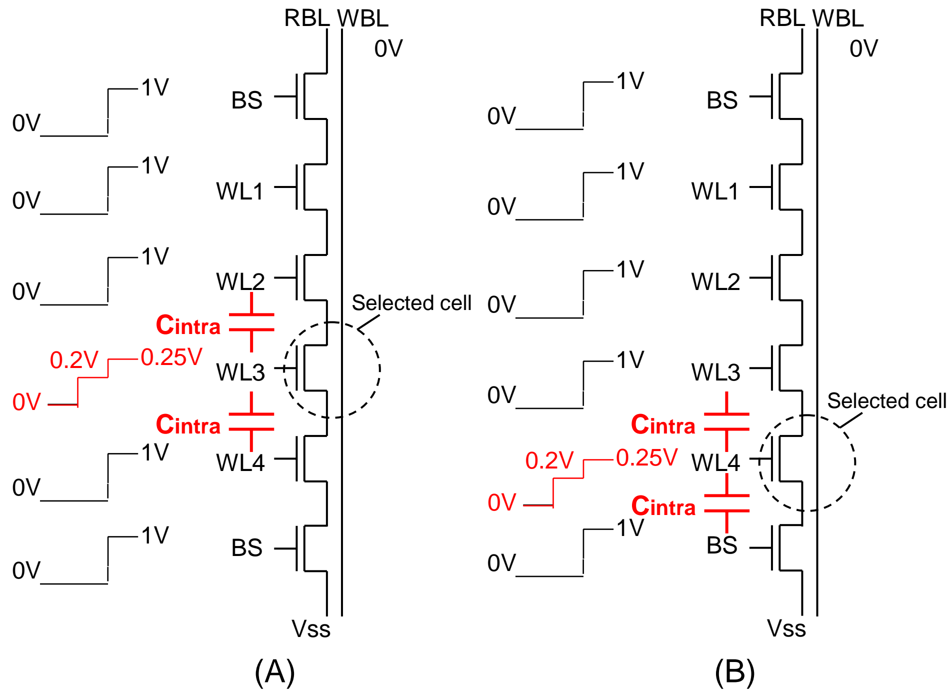

Figure 10: Novel design scheme which uses the memory cell array noise for generating the signal during read operation for stacked type NAND DRAM. (A)WL3 is selected, (B)WL4 is selected.

For realizing the novel design scheme row decoder circuit, row decoder driver circuit, and timings during read operation must be change from the conventional scheme[2] as shown in Fig.11,12,13. Fig.11 shows the row decoder circuit. Compared with conventional scheme[2], the output of NOR decoder, BSIN, is separated to BS with switching transistor, its gate is ϕ_{WL}. This is because, passed WLs and BS must be activated from 0V to 1V simultaneously. Fig.12 shows the row decoder driver circuit. Compared with conventional scheme[2], 0.2V supply circuit for read is newly adopted for generating V_{LOW}. Using this circuit the selected WL is precharged to 0.2V. Furthermore, by introducing the complimentary clocks ϕ_{PRI} and ϕ_{STORE} the selected WL's level is kept to 0.25V. Fig.13 shows the timings during read operation. In the conventional scheme[2] V_{LOW} and V_{HIGH} are activated at the same time. In the newly proposed scheme V_{LOW} is activated first for the precharge of selected WL to 0.2V. After that V_{HIGH} is activated for the activation of passed WLs and BS. The read sequence of the novel design scheme is as follows. After the activation of address input, X1-X4, V_{LOW} is charged from 0V to 0.2V. After that the selected WL is precharged from 0V to 0.2V. The precharge time is T_{PR}. Then ϕ_{PRI} goes down. Selected WL becomes the floating condition. After that V_{HIGH} are activated from 0V to 1V. Therefore, passed WLs and BS are activated from 0V to 1V.

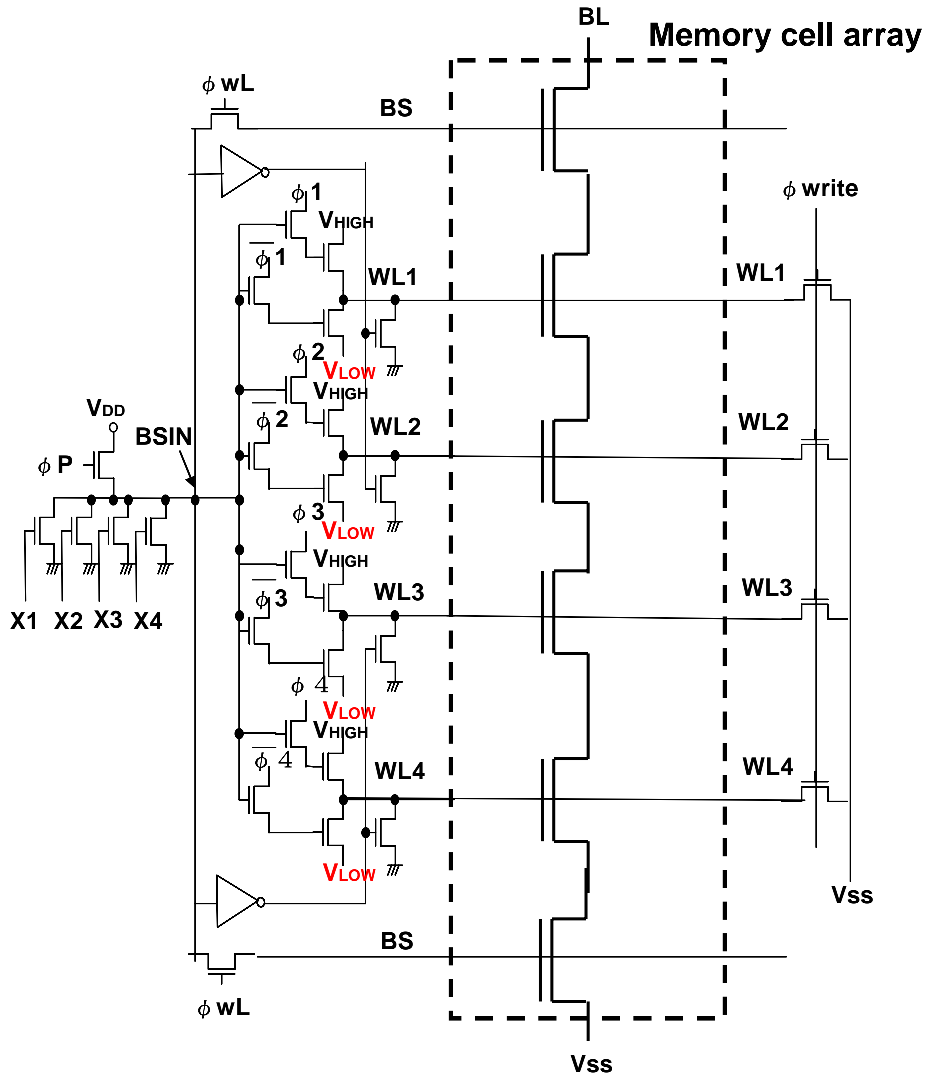

Figure 11: Row decoder circuit for novel design scheme.

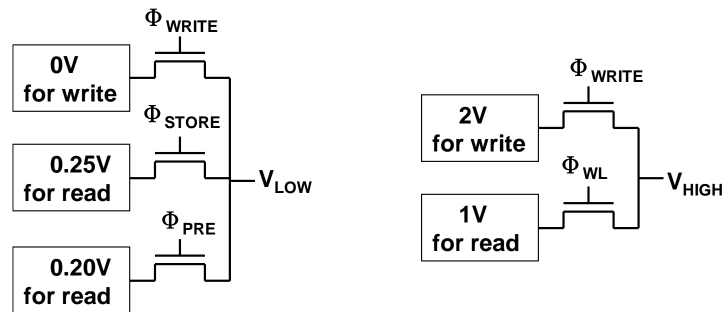

Figure 12: Row decoder driver circuit for novel design scheme.

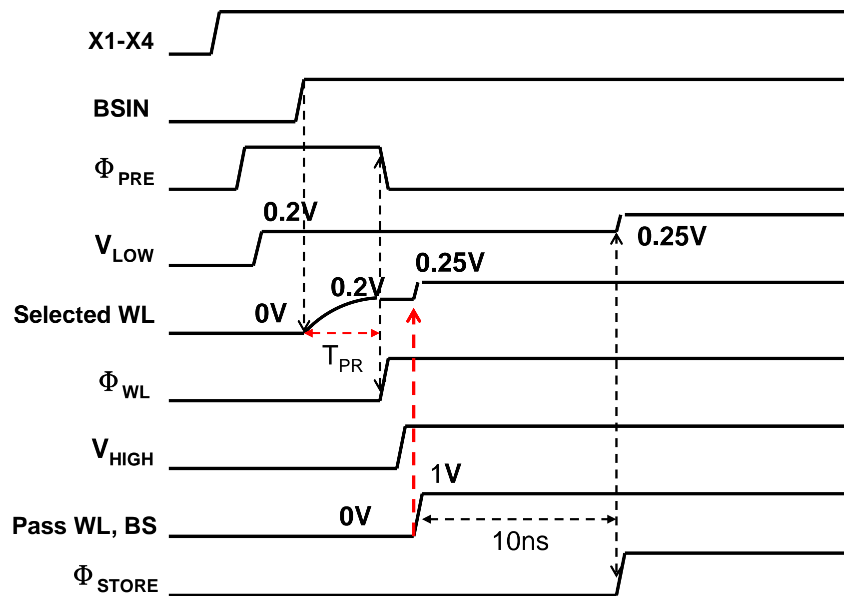

Figure 13: Timings during read operation for novel design scheme.

At the same time the floating selected WL is charged from 0.2V to 0.25V with the assist of capacitance coupling between selected cell to the adjacent passed cell. After 10ns from passed WL and BS activation ϕ_{STORE} is activated for keeping the selected WL's level of 0.25V against the leakage current.

Using this novel design method stable operation can be successfully achieved without reducing the memory cell array noise during read operation. The drawback of this novel design scheme is negligible small penalty of bit cost and access time as follows. For the novel design scheme transistor, its gate signal of BS, must be newly connected in the lowest stage of NAND structure (Fig.10). This causes the increase of process step of 4% compared with 1 layered NAND flash memory[17]. This leads to the increase in bit cost 4/(100+4*16) =0.024=2.4% assuming that 16 layer is adopted[17]. For the novel design method the precharge time of selected WL to 0.2V , T_{PR} in Fig.13, must be added.

This causes increase of access time about WL delay time 2.79ns of the conventional scheme[2]. These results are summarized in Fig.14 compared with noise reduction scheme for εr =2 shown in Fig.9. Not only noise reduction scheme using relatively realistic high-k process of εr =2 but also the novel design scheme described in this section is a promising candidate for realizing stable read operation for stacked type NAND MRAM.

C_{intra} and C_{inter} are not depend on the absolute value of design rule of F but depend on ratio (WL thickness)/(distance between adjacent WLs). Therefore, the newly proposed novel design scheme can be used for further small design rule. If the small difference between $\Delta V_{N\ READ\ MAX}$ to 50mV for selected WL signal is occurred, this small difference can be compensated with controlling passed WL

voltage of 1V or prechage voltage of selected WL of 0.2V.

	Conventional scheme	Proposed noise reduction scheme	Proposed novel design scheme
	ε_r=3.9	ε_r=2	ε_r=3.9
ΔVN READ MAX	48mV	Less than 10mV	48mV
Distance between WLs	F	3F	F
Bit cost	1	1.14	1.024
additional delay time	0ns	2.58ns	2.79ns
New process/ circuit technology	──	Process for Low k	Additional circuit to row decoders
Read operation	Mal-function	Stable operation	Stable operation

Figure 14: Summary of newly proposed novel design scheme with the noise reduction scheme as a reference.

5 Conclusion

In this paper design scheme considering memory cell array noise for stacked type NAND MRAM has been newly described. Memory cell array noise which is inherent to stacked type NAND MRAM is newly analyzed. This noise for read operation of 48mV is almost equal to the signal to selected WL of 50mV during read operation. 3 kinds of design method, the increase in distance between adjacent WLs, introduction of high-k insulating layer, and air gap, which can reduce the memory cell array noise has been newly proposed. Furthermore, the novel design method which uses the memory cell array noise caused by the conventional scheme for generating the signal of 50mV has been newly proposed. These proposed schemes are promising candidates for realizing stable operation of stacked type NAND MRAM.

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