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Study of Pattern Area of Logic Circuit with Tunneling Field-Effect Transistors

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Abstract

The study of pattern area of logic gates, such as NAND gates and full adder circuit with planar and 3 dimensional structure of TFET has been newly described. It is newly observed that extra pattern area for connecting between adjacent N+/P+ diffusion layer is required for designing logic circuit such as NAND/NOR gates. This extra pattern area is newly observed for designing not inverter circuit but NAND/NOR gates. This extra pattern area can be reduced by introducing independent-gate controlled 3 dimensional double gate transistor because of the reduction of number of transistor connected in series. The reduction of this extra pattern area is key technology for designing TFET equivalent to the increased mirror capacitance and unidirectional current flow.

Keywords: TFET, FinFET, double gate, pattern area, LSI, logic circuit

1 Introduction

Over the past decades, CMOS technology has been scaled down aggressively in order to increase integration density, operation speed and energy efficiency. However, MOSFETs have fundamental limit of 60mV/decade sub-threshold swing (SS) at room temperature. With this large SS value minimizing power consumption with small supply voltage while maintaining high on current is a contradictory requirement. Switching mechanisms that can achieve less than 60mV/decade in a FET structure include tunneling [1] [2], impact ionization [3] and mechanical gates [4]. In these candidates the tunneling field-effect transistor (TFET) is the most promising candidates. This is because it can be controlled at volts well under a volt and dose not have the delays associated with positive feedback that are intrinsic to impact ionization and mechanical mechanisms [5].
There are many reports about device technology for TFET such as the enhancement of high on current (enhancement of mobility) [6] [7], reduction of SS [8] [9], and introduction of 3 dimensional structure of TFET [10][11]. On the other hand, reports about circuit technology of TFET are limited to the inverter level. Only estimation of performance for a chain of inverter with inherent increased miller capacitance [12] and circuit design of SRAM cell composed of 2 inverters and 2 transfer transistors which is inherent to unidirectional current flow [13][14][15] have been reported. There is no report about circuit technology for NAND and NOR gates with TFET. And also, the circuit technology with TFET is limited to planar transistor structure. There is no report about circuit technology with 3 dimensional structure of TFET.
In this paper, the study of pattern area of logic gates, such as NAND gates and full adder circuit with planar and 3 dimensional structure of TFET has been newly described. This paper is organized as follows. Section 2 describes the structure of transistors and features of pattern layout for TFET. Section 3 describes the pattern layout of logic circuit such as inverter and NAND gates. Section 4 presents the pattern layout of full added circuit. Finally, a conclusion of this work is provided in Section 5.

2 Structures of transistors and features of pattern layout for TFET

The structure of estimated nMOS transistors in this paper is shown in Fig.1. Fig.1 (a)(c)(e) are the conventional MOS transistor which is featured with same polarity of source/drain electrodes (N+ for source and N+ for drain). Fig.1 (b)(d)(f) are TFET which is featured with different polarity of source/drain electrodes (P+ for source and N+ for drain). For connecting adjacent transistor’s source to drain with

different polarity, extra pattern area (extra pattern area) should be introduced within nMOS area as shown in Fig.2 ①. This extra pattern area is consisted with contacts to N+ and P+ diffusion layer and wiring (isolation of diffusion layer) between these two contacts. As the same as nMOS case, PMOS TFET uses different polarity of source/drain electrode (N+ for source and P+ for drain). Therefore, extra pattern area will be introduced within PMOS area as shown in Fig.2 ②. On the other hand, for connecting drain to drain with different polarity between nMOS to PMOS extra pattern area is not required. This is because this connecting part is included within the well isolation area as shown in Fig.2 ③.
Fig.1 (a)(b) are the conventional planar transistors. Fig.1 (c)(d) are 3 dimensional FinFET which is planning to use high end MPU [16][17]. Fig.1 (e)(f) are 3 dimensional independent-gate controlled double gate transistors [18][19]. This double gate transistor is featured with reduction of the number of transistors connected in series compared with that of planar transistor and FinFET. This feature leads to the reduction of the number of connection which leads to the extra pattern area as described in section 3.

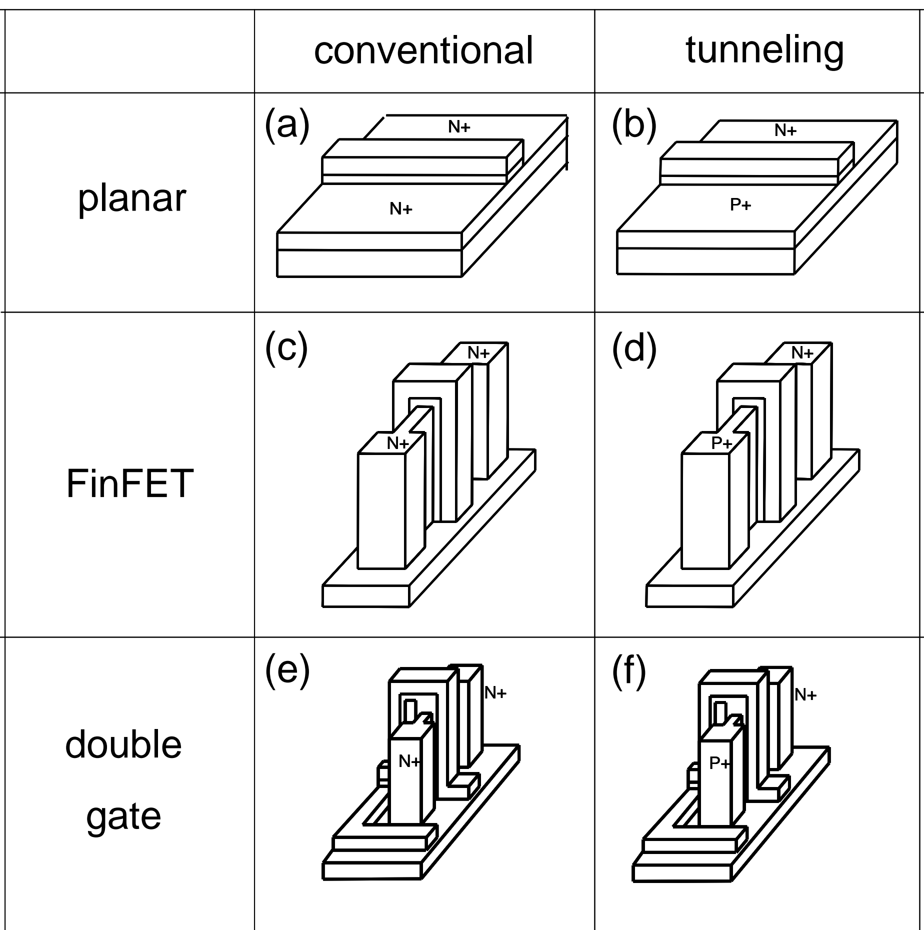

Figure 1: Structure of estimated transistors.

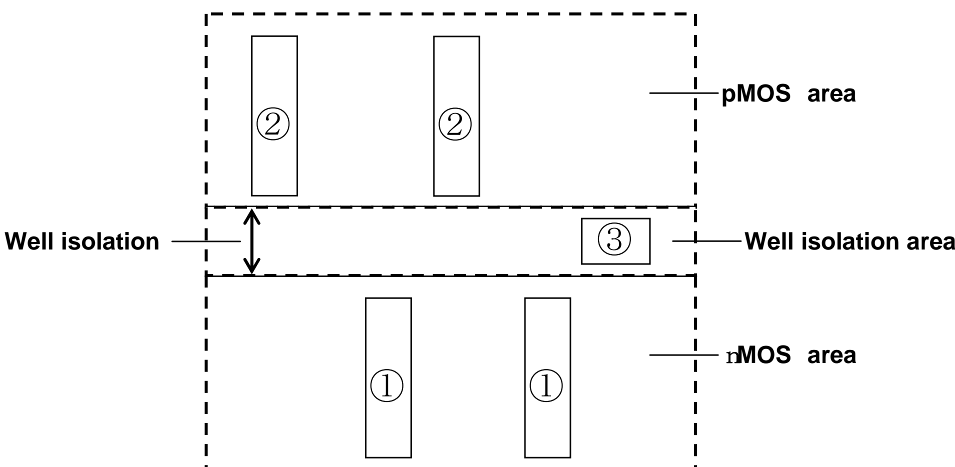

Figure 2: Schematic diagram of layout pattern for TFET.

3 Pattern layout of logic circuit(inverter and NAND gates)

Layout pattern of logic circuit, inverter and NAND gates, using the transistors of Fig.1 is designed with the design rule as shown in Table.1. F is feature size. In this study it is assumed that the same drain current flows, if the gate length, the channel width, and applied voltage are the same value. The channel width is 10F.

Table 1: Design rule.

	Planar	FinFET	Double gate
Gate length	F	F	F
Wiring	F	F	F
Wiring to Wiring	F	F	F
Well isolation	3F	3F	3F
Contact size	F×F	F×F	F×F
Width of planar gate	—	F	—
Sidewall channel width	—	4.5F	10F

Layout pattern of inverter circuit using transistor of Fig.1 (a)(b)(d)(f) is shown in Fig.3. It is notable that the pattern area of (b) is the same as that of (a) in spite of different N+/P+ source/drain structure as described in section 2. This is because as the same as (a) the connecting part between P+ of pMOS and N+ of nMOS is included within the well isolation area as shown in Fig.2 ③. Therefore, previous reports about inverter circuit with TFET did not pay any attention to pattern area. On the other hand, previous report paid much attentions to increased mirror

capacitance [12] and unidirectional current flow [13][14][15] which are indispensable for the inverter circuit and transfer transistor. By using 3 dimensional structure (d)(f) pattern area can be drastically reduced to 33.3% compared with that of (a)(b). The pattern area of (f) is the same as that of (d). For inverter circuit the number of input is only one. Therefore, the feature of double gate structure, reduction of the number of transistors, can not be realized for inverter circuit.

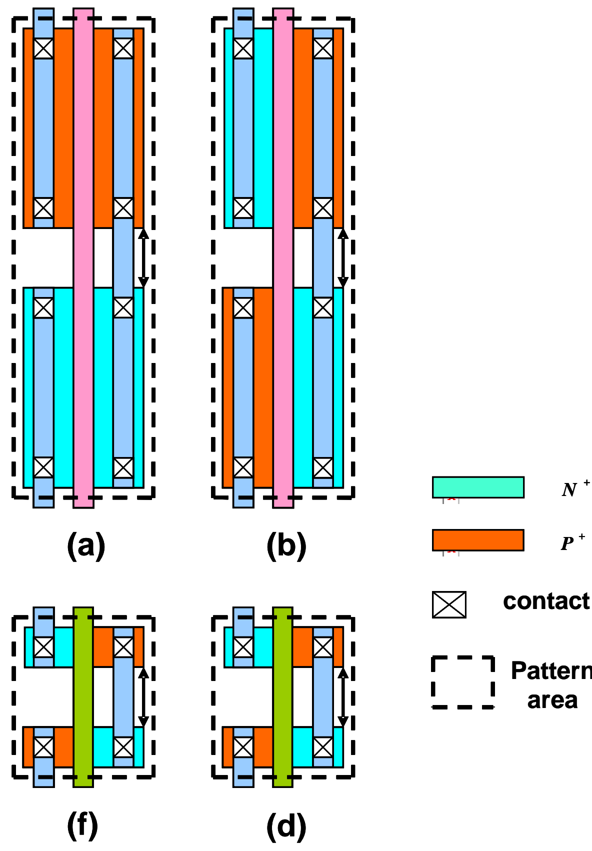

Figure 3: Layout pattern of inverter circuit.

Layout pattern of 2 input NAND circuit using transistor of Fig.1 (a)(b)(d)(f) is shown in Fig.4. It is notable that the pattern area of (b) is by 27.3% larger than that of (a) because of extra pattern area shown in Fig.2 ① as described in section 2. This extra pattern area is newly observed for designing not inverter circuit but NAND gates. The reduction of this extra pattern area is key technology for designing TFET equivalent to the increased mirror capacitance and unidirectional current flow. This extra pattern area can not be eliminated by introducing 3 dimensional transistor sturucture (d). On the other hand, this extra pattern area can be successfully eliminated by introduing 3 dimensional transistor structure (f). This is because using this structure transistors connected in series can be replaced to one independent-gate controlled double gate transistor [18][19]. As a result, the pattern area of (f) can be reduced to 28.5/48.2=59.1% compared with that of (d). This is newly proposed idea for reducing the extra pattern area caused by the

introduction of NAND circuit with TFET. For 2 input NOR circuit the same extra pattern area is necessary for PMOS region as shown in Fig.2 ②. As the same as 2 input NAND circuit case this extra pattern can be eliminated by using one pMOS independent-gate controlled double gate transistor (Fig.6). For NAND circuit and NOR circuit with TFET the effectiveness of independent-gate controlled double gate transistor is increased with increasing the number of input as follows.

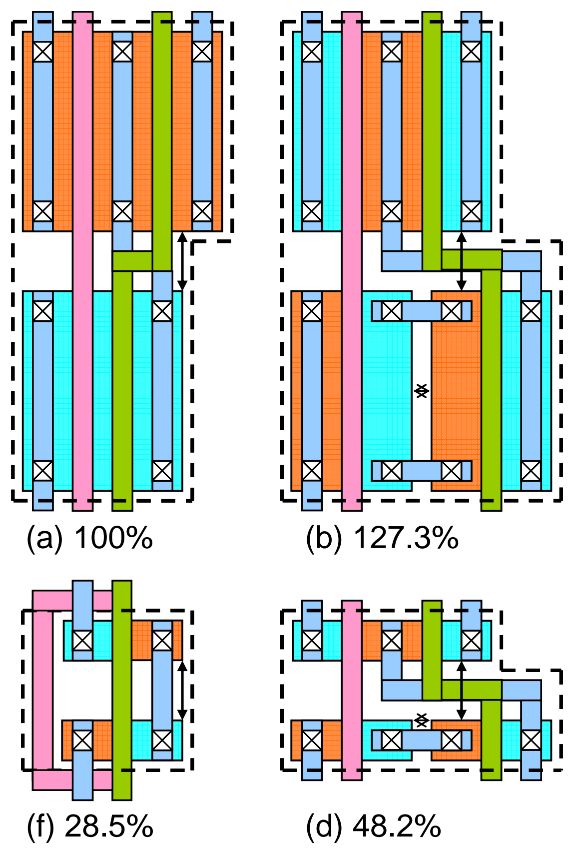

Figure 4: Layout pattern of 2 input NAND circuit.

Layout pattern of 4 input NAND circuit using transistor of Fig.1 (a)(b)(d)(f) is shown in Fig.5. The pattern area of (b) is by 48.4% larger than that of (a). This value is larger than that of 2 input NAND circuit. This is because the number of connection (number of connection) which causes the extra pattern area is increased from 1 to 3. As the same as 2 input NAND case the number of connection can not be reduced by using 3 dimensional transistor (d). As the same as 2 input NAND case the number of connection can be reduced by introducing independent-gate controlled double gate transistor from 3 to 1. This is because 4 transistors connected in series can be replaced to 2 independent-gate controlled double gate transistors connected in series (Fig.6). As a result, the pattern area of (f) can be reduced to 32.9/54.0=60.9% compared with that of (d).

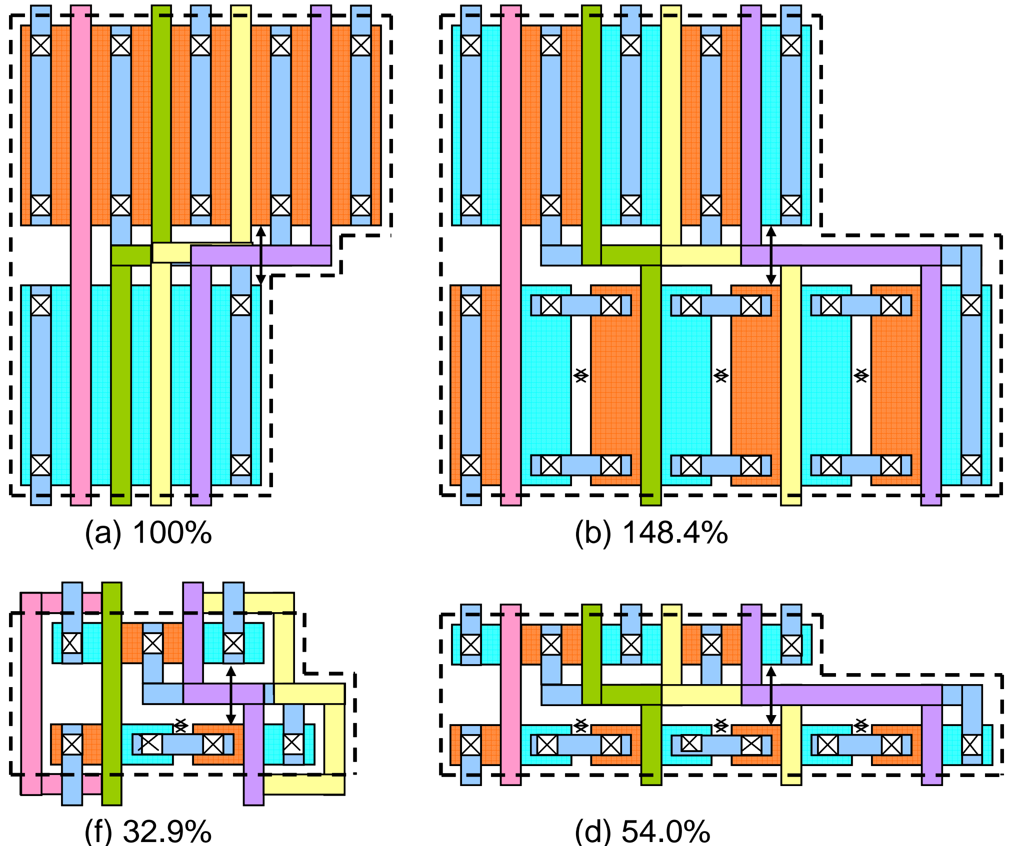

Figure 5: Layout pattern of 4 input NAND circuit.

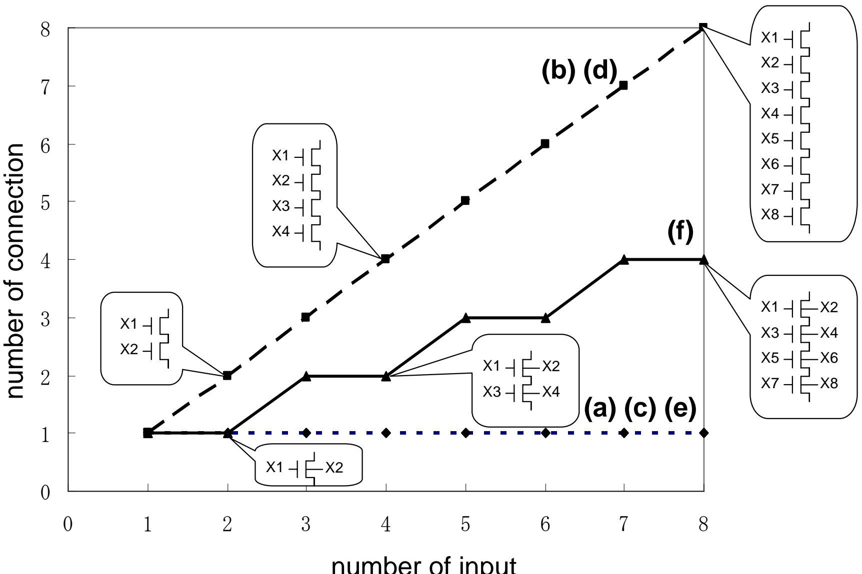

Figure 6: Number of connection dependence on number of input for NAND circuit.

The number of connection dependence on number of input for NAND circuit is shown in Fig.6. The well isolation is taken into account one connection for Fig.6.

For the conventional MOS transistor case (a)(c)(e), the number of connection is one (only well isolation) which is independent to the number of input. This is because (a)(c)(e) are featured with same polarity of source/drain electrodes. By introducing the TFET number of connection is almost proportionally increased for increasing the number of input. The constant of proportionality is 1 for (b)(d) which results in large increase of pattern area. On the other hand, by introducing independent-gate controlled double gate transistor (f) the constant of proportionality can be reduced to 0.5. This leads to smaller increase of pattern area compared with that of (b)(d).
And also this result is summalized as the pattern area in Fig. 7. The pattern area of (a) for 1-4 input is normalized to 100%.

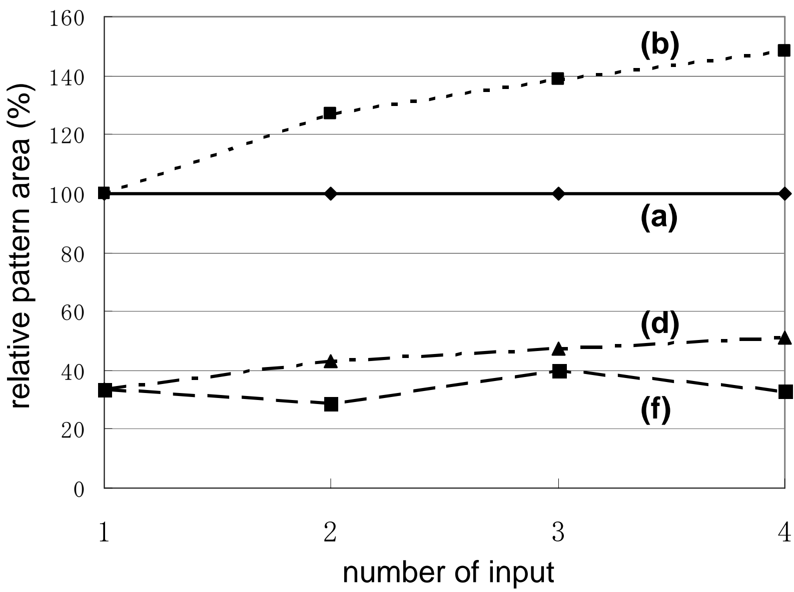

Figure 7: Relative pattern area dependence on number of input for NAND circuit.

4 Pattern layout of full adder circuit

For study of the complex circuit compared with inverter and NAND circuit, full adder circuit, composed with 2 input NAND, 2 input NOR and inverter has be designed. The layout pattern of full adder is shown in Fig.8. The same tendency of pattern area reduction as NAND circuit is observed. The pattern area of (b) is 18.4% larger than that of (a). This value is smaller than that of 2 input NAND or NOR circuit. This is because inverter circuit and wiring region, its pattern area is not increased by introducing TFET, are included within the full adder circuit. For the same reason the pattern area ratio (f) to (d), 53.1/65.8=80.7% is larger than that of 2 input NAND or NOR circuit.

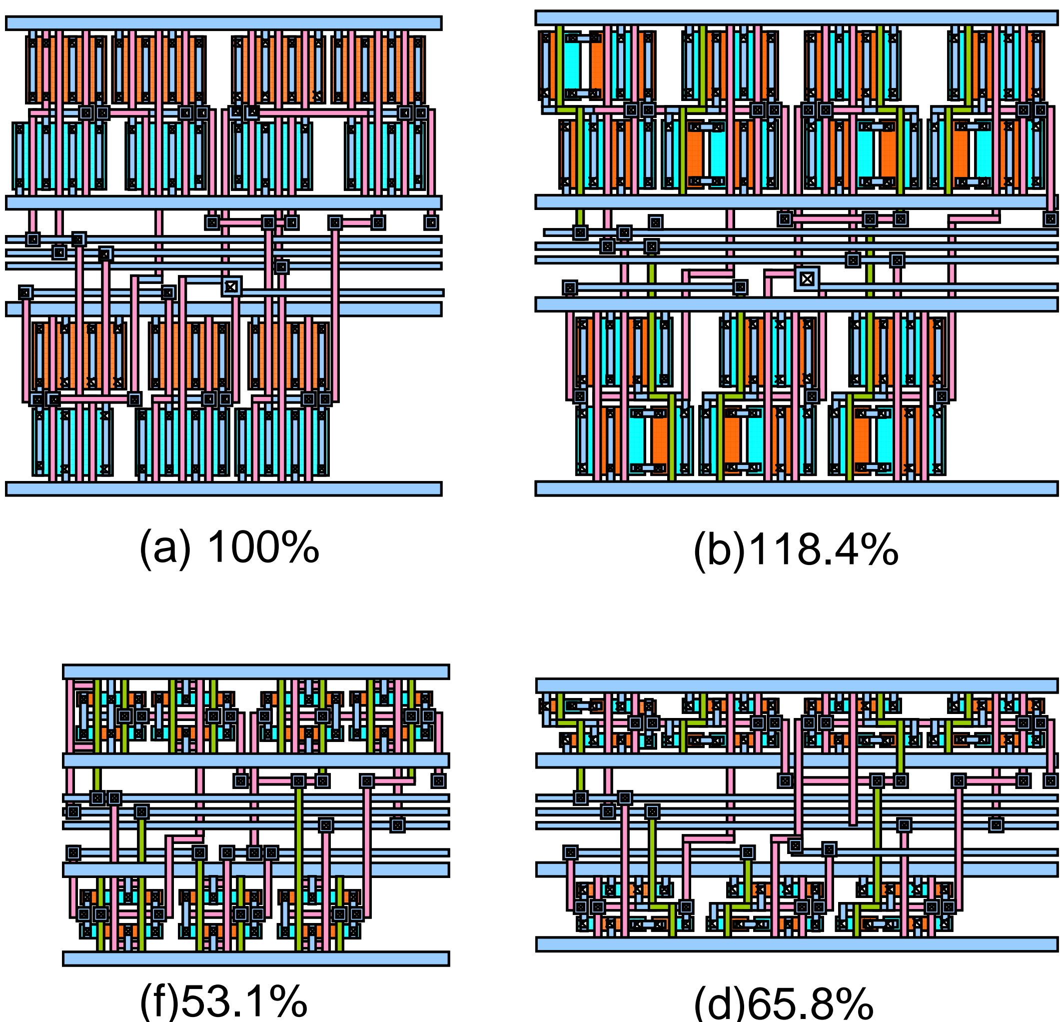

Figure 8: Layout pattern of full adder circuit.

5 Conclusion

Conclusion of this paper is summarized in Fig.9. The study of pattern area of logic gates, such as NAND gates and full adder circuit with planar and 3 dimensional structure of TFET has been newly described. It is newly observed that extra pattern area for connecting between adjacent N+/P+ diffusion layer is required for designing logic circuit such as NAND/NOR gates. This extra pattern area is newly observed for designing not inverter circuit but NAND/NOR gates. This extra pattern area can be reduced by introducing independent-gate controlled 3 dimensional double gate transistor because of the reduction of number of transistor connected in series. The reduction of this extra pattern area is key technology for designing TFET equivalent to the increased mirror capacitance and

unidirectional current flow. Newly proposed scheme is promising candidate for realizing small pattern size logic circuit with TFET.

		Problem	Proposed solutions	
Device	Transistor (TFET)	Small current drivability	Optimization of device design	Previous work
Circuit	Inverter circuit	Increased mirror capacitance	Accurate TCAD simulation	Previous work
Circuit	Transfer gate (SRAM)	Unidirectional current	TFET F/F + MOS transfer 7 transistor memory cell	Previous work
Circuit	Logic circuit (NAND/ NOR gates)	Extra pattern area for connection for N+/P+ diffusion layer	Independent-gate controled Double gate transisitor	This paper

Figure 9 : Summary of this paper

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