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Novel Current Limit Value Test Technology with Voltage-Mode

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Abstract

This paper proposes novel current-limit test technology, which can test current-limit with voltage mode. Current limit value can be realized accurately and efficiently under small current condition with voltage mode. This test technique has high anti-noise capability, high stability, low cost and saves test time because it avoids high current input.

Keywords: current limit value, voltage mode, anti-noise, high current input

1 Introduction

With more and more power devices are integrated, how to test power device current limit accurately, fast and economically during mass production becomes a big challenge. [1-3]. Traditional technique of current limit test is measuring real current value directly with current mode. This method has two main disadvantages: 1) A real limit current is needed during test and it is easy to introduce noise 2) When the current peak is too high, it is very difficult to measure accurate current limit value [4-5].

2 Testing current limit value with voltage mode

In order to solve major drawbacks of direct measurement of current limit value with current mode. A new efficient current-limit test technology is proposed in this paper, as shown in Fig.1. The test techniques can be divided into two test steps: The first step is to test effective sensing resistor RSENSE through a small current source. The second step is to test the required voltage V_{t_LIMT} by scanning voltage to the positive terminal of current limit comparator directly.

2.1 Test technique for sense resistor value

The effective sense resistor test method is shown in Figure 2. Pin IFB is forced to connect the upper terminal of sense resistor by Kelvin connection, meanwhile, pin ISET is forced to connect the output pin PGND which is source of power MOSFET by Kelvin connection. If the ratio of chip power MOSFET and mirror power MOSFET is K, then:

$$V_{SENSE} = (\frac{R_S \times R_0}{K \times R_0 + R_S} + R_{pm}) \times I_{test} \tag{1}$$

$$R_{SENSE} = \frac{V_{SENSE\,2}}{I_{test}} = \frac{R_S \times R_0}{K \times R_0 + R_S} + R_{pm} \tag{2}$$

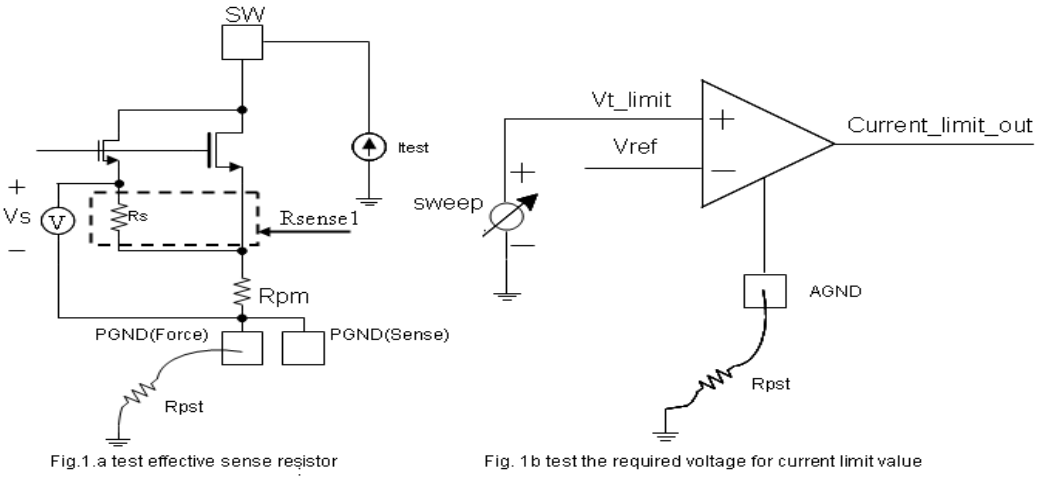

Fig.1 principle schematic of testing current limit value with voltage mode

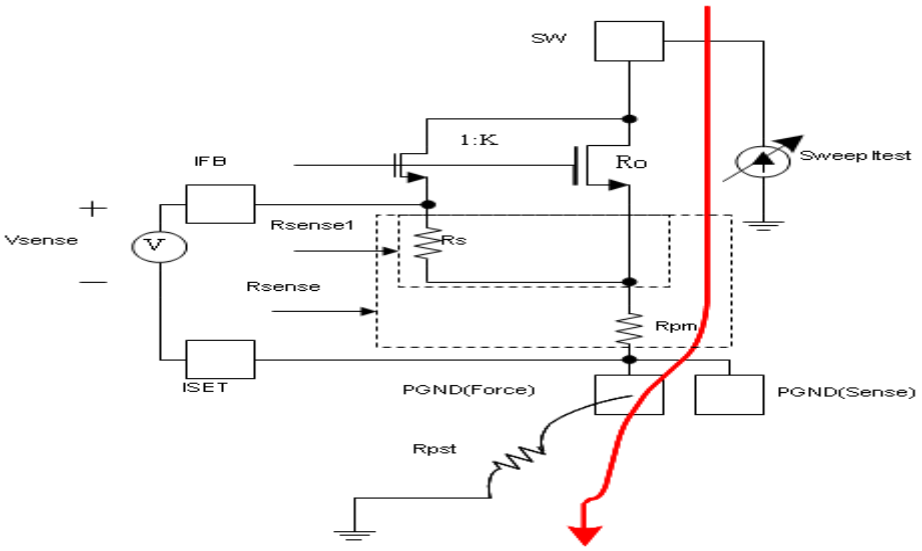

Fig.2 test schematic about sense resistor value

In equation (2), R_S denotes the original sense resistor, R_0 denotes the R_{dson} of power mosfet, R_{pm} denotes the parasitic resistance of metal trace. R_{SENSE} denotes the effective design sense resistor. As parameter R_S, K, and R_{pm} are almost fixed constant, the effective designed sense resistor R_{SENSE} is almost irrelevant with the input test current .Therefore, R_{SENSE} can be measured accurately even testing current is small.

2.2 test technique for voltage-mode current limit value

Voltage-mode current limit test technique is shown in Figure 3. A scanning voltage is sent to the positive terminal of the current limit comparator, when

$$V_{t\_limit} = V_{ref} \tag{3}$$

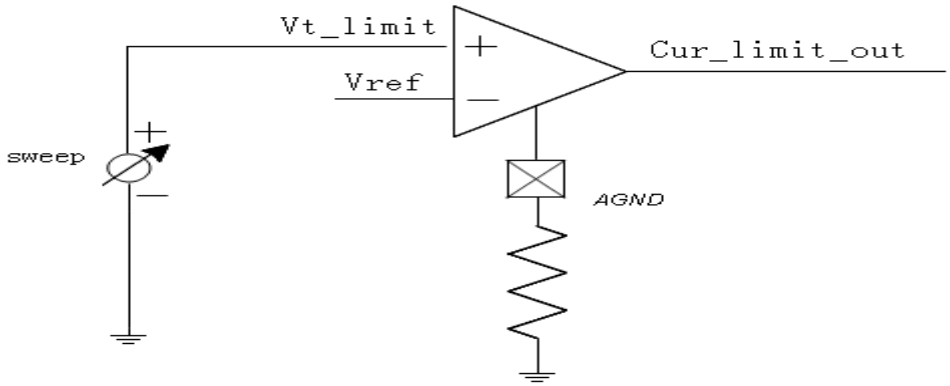

Fig.3 principle schematic for the required voltage of current limit value

The output of current limit comparator is changed from low to high. At this point, the scanning voltage is equivalent to effective sense voltage when there appears a current limit value under normal operation.

Therefore, according to equation (2) and (3) current limit value can be easily calculated as follows:

$$I_{Limit} = \frac{V_{ref}}{\frac{R_S \times R_0}{K \times R_0 + R_S} + R_{pm} + R_{pb}} \tag{4}$$

3 Summary

A novel current limit test technique is proposed in this paper. Compared to traditional current mode method, this method avoided input real high current in test mode at chip level, reduced the introduced noise under the high current test condition, improved test accuracy of current limit value and decreased test cost and time.

References

[1] Marty Brown, Practical Switching Power Supply Design, Acedemic Press, Inc. Copyright 1990.

[2] P. J. Carlson, Reliability implications in using intelligent power integrated circuits (PICs) , Proceedings of Power Conversion, 1989, 450-454.

[3] Abraham. I. Pressman, Switching Power Supply Design, McGraw-Hill, Inc. Copyright 1991.

[4] Robert Mayell and E.H. Quek, An Integrated Switching IC Incorporating an Innovative Feedback Method for Switching Power Supplies, IIC, China, April, 1999.

[5] Texas instruments, 3-A High Voltage Boost Converter with Soft Start and Programmable Switching frequency, Texas instruments 2008.

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