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# Study of Chip Cost of LSI Using FinFET with Plural Number of Sidewall Channel Width

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**Abstract**

Study of chip cost of LSI using FinFET with plural number of sidewall channel width is newly described. Using the sequential fabrication of 3-4 kinds of sidewall channel chip cost of buffer circuit and CMOS cell library can be reduced by 5-5.7% compared with of that with conventional single number of sidewall channel width. Further reduction of chip cost can be realized by using simultaneous fabrication process. LSI using FinFET with plural number of sidewall channel width is promising candidate for realizing low cost high density LSI. Furthermore, simultaneous process has the possibility to change the presently available CAD technology for LSI drastically.

**Keywords**: FinFET, trench depth, sidewall channel width, pattern area, chip cost, LSI

## 1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem FinFET which use the 3 planes as the channel for reducing the short

channel effect has been developed [2][3]. By using FinFET not only reduction the short channel effect but also the reduction of the pattern area compared with those of the conventional planar transistor can be realized [4]. This is because not only the planar region but also the sidewall can be used as the channel. The structure of FinFET is shown in Fig.1. Within the small pattern area large total channel width of $W_P$+2$W_D$ can be successfully realized. Because of these features Intel firstly produces FinFET on commercial basis as the high end CPU this year [5][6].

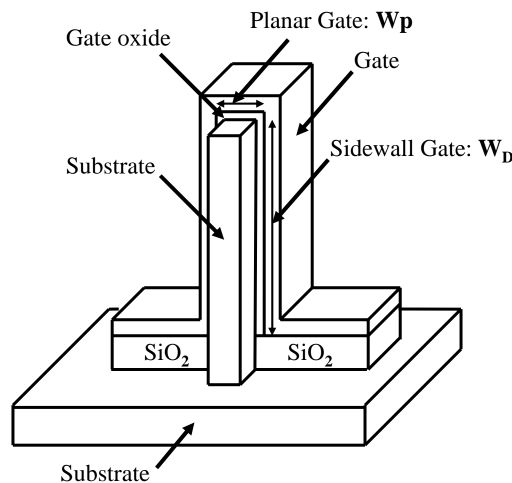


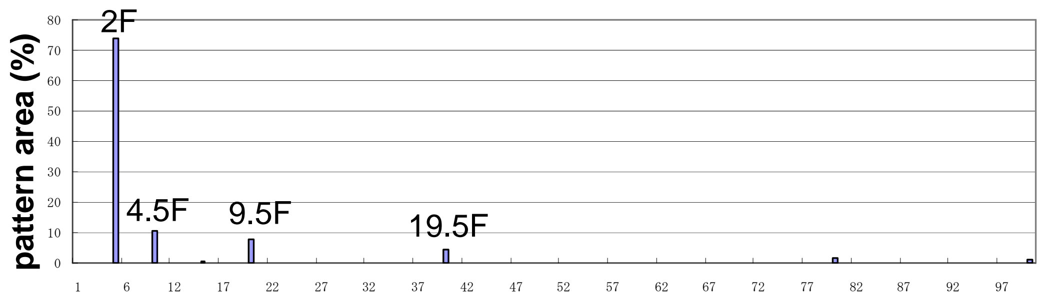

Figure 1: Structure of FinFET

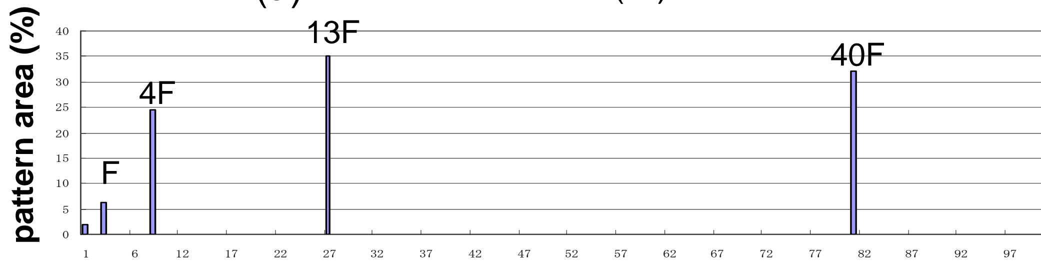
The research of LSI with FinFET is focused on the operation speed and the power consumption. The research of LSI with FinFET about the pattern area is very few [4][7]. In these researches about pattern area only one kind of sidewall channel width is adopted within a LSI for simplify the process technology [4]. The plural number of sidewall channel width within a LSI is not reported for avoiding the complexity of circuit and process technology. In this paper, the study of LSI for FinFET with the plural number of sidewall channel width in order to reduce the pattern area has been newly described. Furthermore, chip cost, fabrication cost of 1 chip, is also described.

This paper is organized as follows. Section 2 describes the 3 types of LSI used in this paper focusing on the distribution of pattern area vs. channel width of the conventional planar transistor. Section 3 presents the reduction of pattern area and chip cost of 3 types of LSI with the plural number of channel width using sequential formation of sidewall channel (sequential process). Section 4 describes further reduction of pattern area and chip cost with simultaneous formation of sidewall channel (simultaneous process). Finally, a conclusion of this work is provided in Section 5.

# 2 Distribution of pattern area vs channel width for 3 types of LSIs

The distribution of pattern area vs channel width of the conventional planar transistor for 3 types of LSIs is shown in Fig.2. Channel width is normalized by the feature size F.



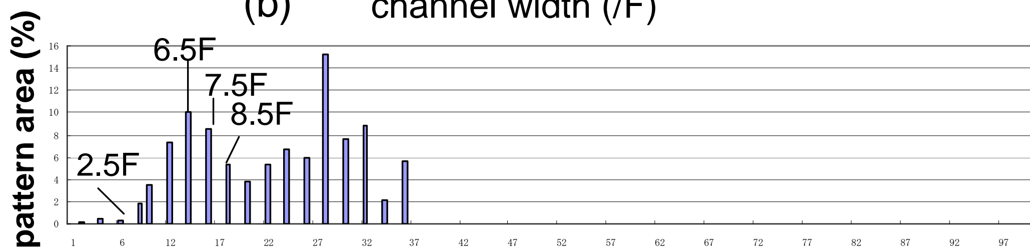




Figure 2: Distribution of pattern area vs channel width of the conventional planar transistor for 3 types of LSIs, (a)LSI for communications, (b)buffer circuit, (c)CMOS cell library

Fig.2 (a) shows the distribution of LSI for communications [8]. With increasing the channel width, the pattern area decreases monotony. This is because smaller power consumption compared with higher speed is important for LSI for communication. Furthermore, the range (width) of channel width for large pattern area is small.

Fig.2 (b) shows the distribution of LSI for buffer circuit [9]. With increasing the channel width, the pattern area increases monotony. This is because high speed

operation is important for buffer circuit. Furthermore, the width (range) of channel width for large pattern area is large compared with that of F.g.2 (a).
Fig.2 (c) shows the distribution of LSI for CMOS cell library [10]. With increasing the channel width, the pattern area increases and reaches to the maximum value and decreases. This distribution is complicated compared with that of Fig.2 (a) and Fig.2 (b). This is because is various kinds of circuits are included in CMOS cell library. The width (range) of channel width for large pattern area is large compared with that of F.g.2 (b).
As shown in Fig.2 the distribution of pattern area vs channel width is different among 3 types of LSIs because of the difference in the functions to be realized. This difference will lead to the different effect of the reduction of pattern area with FinFET.

# 3 Reduction of pattern area and chip size of 3 types of LSIs with sequential process

As described in section 1, the channel width of FinFET is $W_P+2W_D$. For the Wp, feature size, F, is used. The pattern area with FinFET is reduced to $W_P/(W_P+2W_D)$ compared with that of with the conventional planar transistor. In the discussion of this paper it is assumed that for both FinFET and conventional planar transistor the same drain current flows, if the same value of channel width, gate length, and applied voltage are adopted. In the previous works, it is assumed that the value of sidewall channel width of FinFET is only one within a chip for avoiding the complexity of the circuit design and process technology. As a result, the reduction of pattern area with FinFET has limitation for the LSI with wide range of channel width with conventional planar transistor.

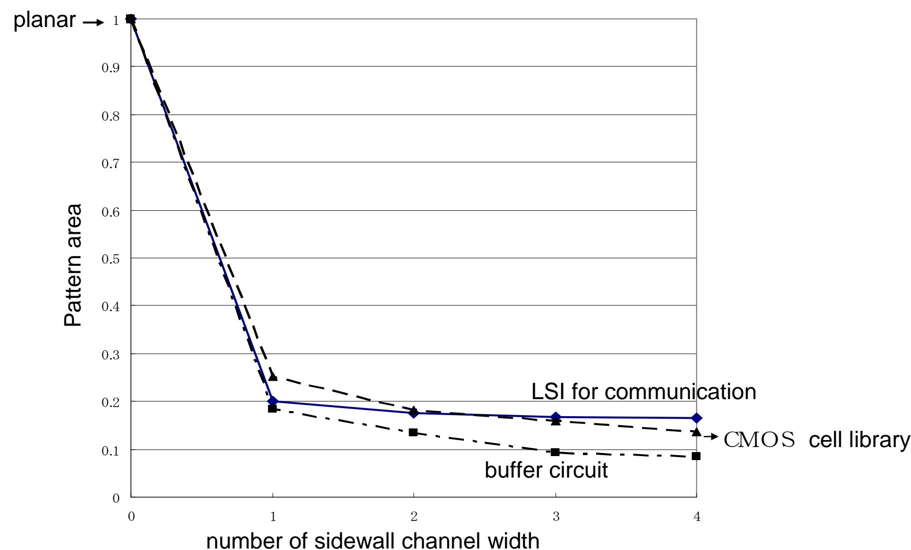



Figure 3: Pattern area dependence of LSI on number of sidewall channel width

In order to overcome this problem technique with the plural number of sidewall width is adopted in this section. As increasing the number of sidewall channel width, N, it is expected that the pattern area of LSIs can be reduced monotony. The estimated result is shown in Fig.3. The value of sidewall channel width is determined so as to realize the minimum pattern area of LSIs for given N. The large reduction of pattern area occurs when N=1 is adopted. The reduction ratio of pattern area increases with increasing N. However, this reduction ratio depends strongly on the type of LSIs. The reduction ratio is largest for CMOS cell library and is smallest for LSI for communication. This result shows that wide width of distribution of channel width causes large reduction rate of pattern area. For 3 LSI cases the pattern area can be reduced drastically with N=4.

Table 1: Pattern area dependence of LSI on number of sidewall channel width ,N

| | LSI for communication | | buffer circuit | | CMOS cell library | |
|---|---|---|---|---|---|---|
| **N** | **pattern area** | **Sidewall channel width** | **pattern area** | **Sidewall channel width** | **pattern area** | **Sidewall channel width** |
| 0 | 1 | | 1 | | 1 | |
| 1 | 0.2 | 2F | 0.184 | 4F | 0.253 | 2.5F |
| 2 | 0.175 | 2F,4.5F | 0.134 | 4F,13F | 0.182 | 2.5F,6.5F |
| 3 | 0.167 | 2F,4.5F,9.5F | 0.093 | F,4F,13F | 0.158 | 2.5F,6.5F,7.5F |
| 4 | 0.165 | 2F,4.5F,9.5F,19.5F | 0.085 | F,4F,13F,40F | 0.136 | 2.5F,6.5F,7.5F,8.5F |

Precise result is shown in Table 1. The pattern area dependence on N and sidewall channel width for each N is surmarized in this table. The values of the pattern area and the sidewall channel width corresponds to the minimization of the pattern area for given N. These values of sidewall channel width are indicated within the Fig.1. In the case of N=1, the value of sidewall channel width for minimizing the pattern area is relatively small (2F for communication, 4F for buffer, 2.5F for cell library). In this case for realizing the larger channel width parallel connection of FinFET with this relatively small value is adopted. As increasing N, the value of sidewall channel width for minimizing the pattern area increases. This tendency is clear for LSI for communication and CMOS cell library. On the other hands, for buffer circuit for realizing large N of 3 or 4, small value of sidewall channel width of F is also employed. These features are strongly depend on the distribution of pattern area vs channel width for conventional planar case.

It is well known that the chip cost of LSI, fabrication cost for 1 chip, is proportional to pattern area and the number of process steps and inversely proportional to the Yield. Therefore, if the increase of process steps due to the fabrication of plural number of sidewall channel width is negligibly small, the chip cost is mainly corresponds to the pattern area. This leads to the reduction of

chip cost with increasing in N. However, the increase of process steps can not be actually neglected for the process technology with sequential formation of sidewall. The increase of process steps for fabricating one sidewall channel width is about 1%-5% [5]. In the actual fabrication of sidewall, trench is fabricated. The value of sidewall channel width is almost the same value as trench depth for this fabrication technique. Therefore, for realizing the N kinds of sidewall channel width, trench formation of different trench depth must be sequentially repeated N times. As a result, for realizing the N kinds of sidewall channel width (1%-5%)*N process steps should be added. The chip cost is estimated the reduction of pattern area and this increasing of process steps taken into account. It is assumed that the reduction of yield due to increasing of process step is negligible small as small as N=4-5 is considered.

Chip cost dependence of LSI for communication on N is shown in Fig.4 (A). Enlarged figure near the optimal point of Fig.4 (A) is also shown in Fig.4 (B).

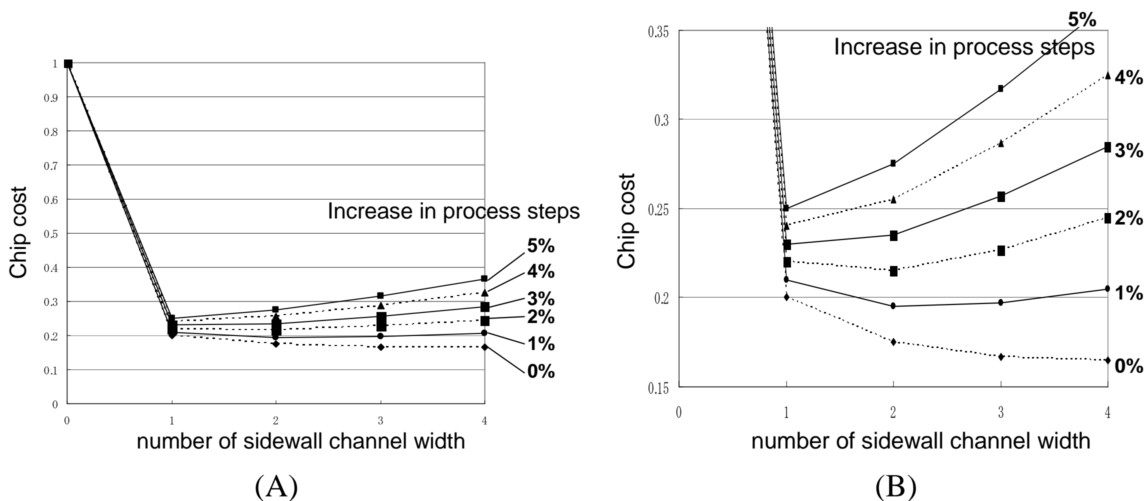
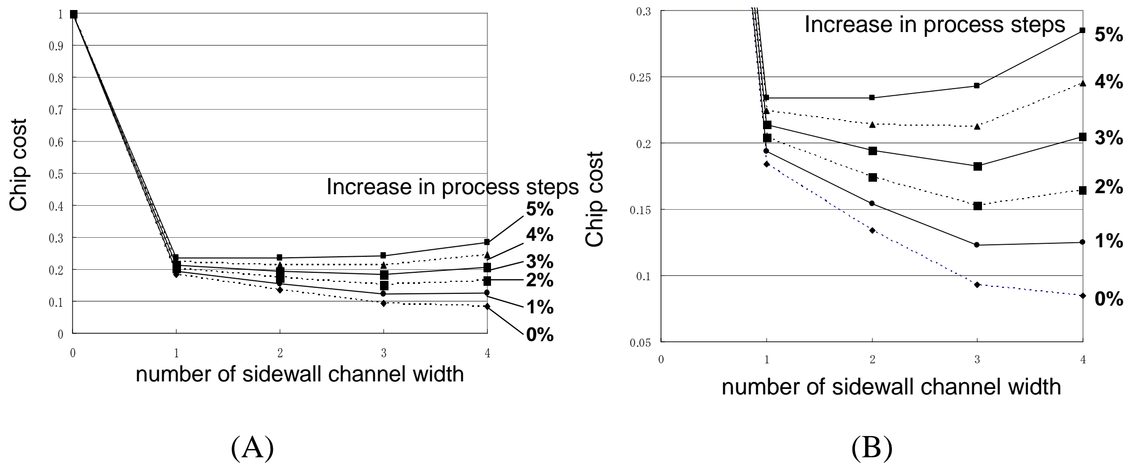



Figure 4: Chip cost dependence of LSI for communication on number of sidewall channel width, N

The chip cost cannot be easily reduced with increasing N. In the increasing in process steps is 2% case, the chip cost becomes minimum value of 0.22 when N=2. This small value of N=2 is caused, because the reduction of pattern area with increasing N is smallest among 3 types of LSIs. This leads to the increase of chip cost with increasing of process steps due to increasing in N.

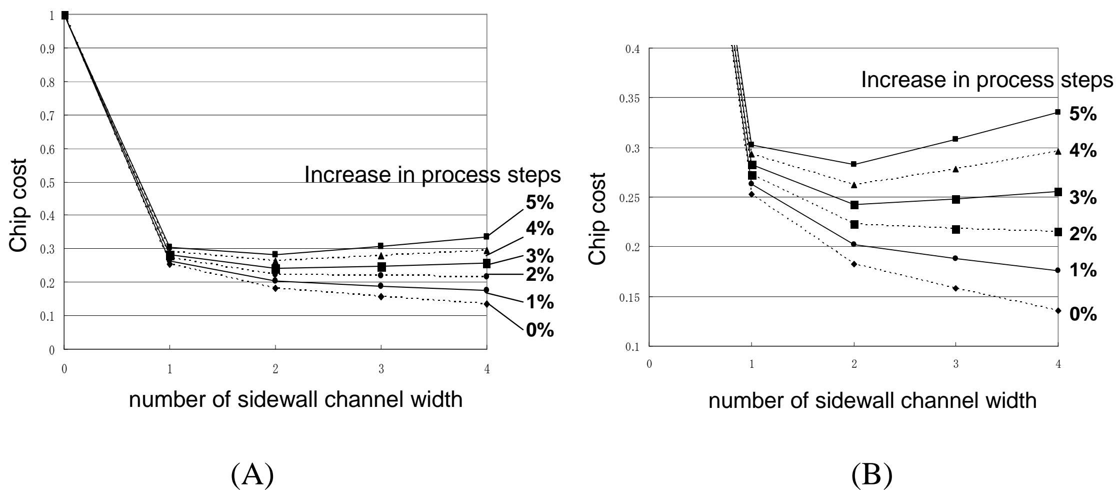
Chip cost dependence of buffer circuit on N is shown in Fig.5 (A). Enlarged figure near the optimal point of Fig.5 (A) is also shown in Fig.5 (B). The chip cost can be reduced with increasing N. In the increasing in process steps is 2% case, the chip cost becomes minimum value of 0.155 when N=3. This value of N=3 is caused, because the reduction of pattern area with increasing N is larger than that of communication. This corresponds to the fact that the width (range) of channel width for large pattern area is large compared with that of communication.




(A) (B)

Figure 5: Chip cost dependence of buffer circuit on number of sidewall channel width, N

Chip cost dependence of CMOS cell library on N is shown in Fig.6 (A). Enlarged figure near the optimal point of Fig.6 (A) is also shown in Fig.6 (B). The chip cost can be easily reduced with increasing N. In the increasing in process steps is 2% case, the chip cost becomes minimum value of 0.205 when N=4. This value of N=4 is caused, because the reduction of pattern area with increasing N is largest among 3 types of LSIs. This corresponds to the fact that the width (range) of channel width for large pattern area is largest among 3 types of LSIs.




(A) (B)

Figure 6: Chip cost dependence of CMOS cell library on number of sidewall channel width, N

Table 2: Chip cost dependence of LSI on number of sidewall channel width. The increase of process steps is 2%.

| | LSI for communication | buffer circuit | CMOS cell library |
|---|---|---|---|
| Optimum number of sidewall channel width | 2 | 3 | 4 |
| minimum chip cost | 0.22 | 0.155 | 0.205 |
| Chip cost (N=1) – minimum chip cost | 0.50% | 5.10% | 5.70% |

The estimated result is surmalized in Table 2. By using the plural number of sidewall channel width with sequential process, N, 0.50-5.70% smaller chip cost compared with that of N=1 can be realized. The reduction rate of chip cost and optimum number of sidewall channel width is strongly depend on the distribution of pattern area vs channel width for conventional planar case. Wider distribution of pattern area leads to larger N and smaller chip cost. Newly proposed FinFET with the plural number of sidewall channel width with sequential process is promising candidates for realizing low cost high density future LSI.

# 4 Further reduction of pattern area and chip cost with simultaneous process

In section 3 by using the FinFET with the plural number of sidewall channel width with sequential process, the reduction of pattern area and chip size can be successfully realized. However, because trench which corresponds to sidewall channel width is fabricated N times sequentially, the effect of chip cost reduction is limited to 5% level because of large increase of process steps.

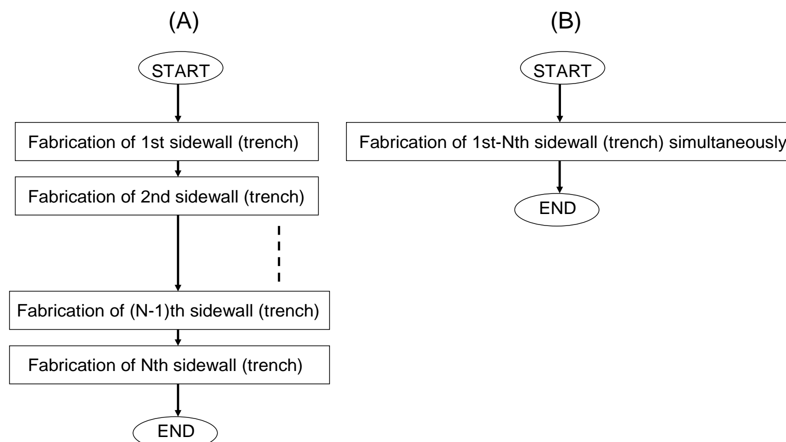



Figure 7: Process steps for fabricating N kind of sidewall (trench), (A)Sequential process used in section 3, (B) Newly proposed simultaneous process used in section 4 which features fabrication simultaneously.

In order to overcome this limitation, simultaneous process which enable to fabricate the various kinds of sidewall (trench depth) simultaneously has been newly proposed. The process step of simultaneous process is compared with that of sequential process described in section 3 (Fig.7). The most promising candidate for realizing the simultaneous process is process technology with feature of trench etching of silicon substrate. The example of this process is shown in Fig.8 (A)[11]. Using small pattern size which is smaller than the feature size, F, various depth of trench can be successfully fabricated simultaneously with the optimization of trench etching process. As decreasing the pattern size (size of hole pattern), the trench depth decreases monotony. Therefore, if controllable relationship between trench depth which corresponds to sidewall channel width and size of hole pattern which corresponds to the isolation width is stably realized, N kinds of sidewall can be realized simultaneously using this relationship. This relationship is represented as (Isolation width) = f(sidewall channel width). The example is shown in Fig.8 (B) and (C). For fabricating 3 kinds of sidewall channel width, $D_1F$, $D_2F$, $D_3F$, isolation width $f(D_1)$ *F, $f(D_2)$* F, $f(D_3)$ *F are employed.

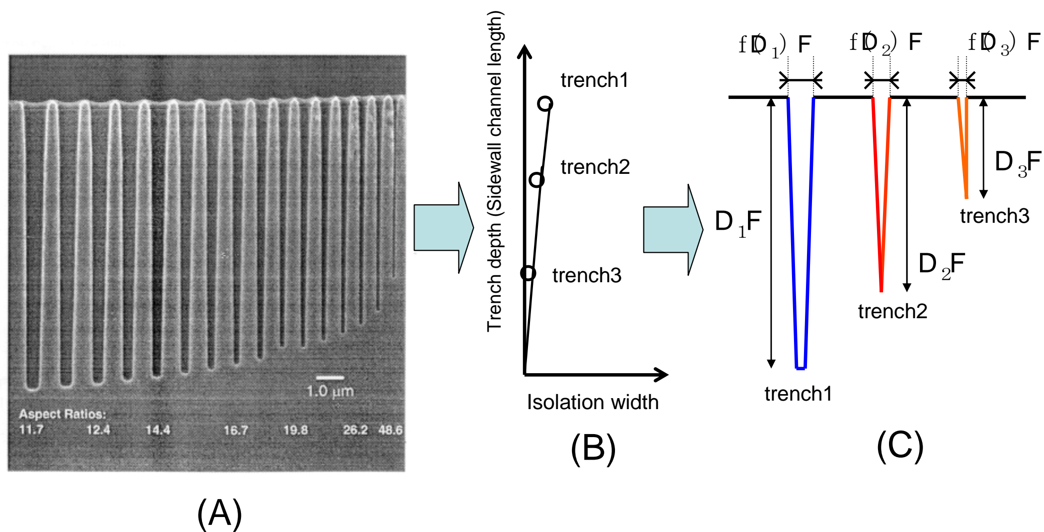



Figure 8: Trench etching process for silicon substrate, (A) Experimental cross sectional view of various depths of trenches fabricated simultaneously, (B) Relationship between sidewall channel width and isolation width, (C) Formation of 3 kinds of trench (sidewall).

The pattern design of a transistor with this simultaneous fabrication process is shown in Fig.9. It is assumed that the channel width is aF. For realizing the sidewall channel width of [(a-1)/2]F, the isolation width of f[(a-1)/2]*F must be fabricated. For this purpose dummy patterns are designed to generate to both side of channel as shown in Fig.9 (B). The distance between the active pattern for FinFET and the dummy pattern is set to f [(a-1)/2]*F. As a result, using the active area pattern for FinFET and dummy pattern which finally becomes dummy active

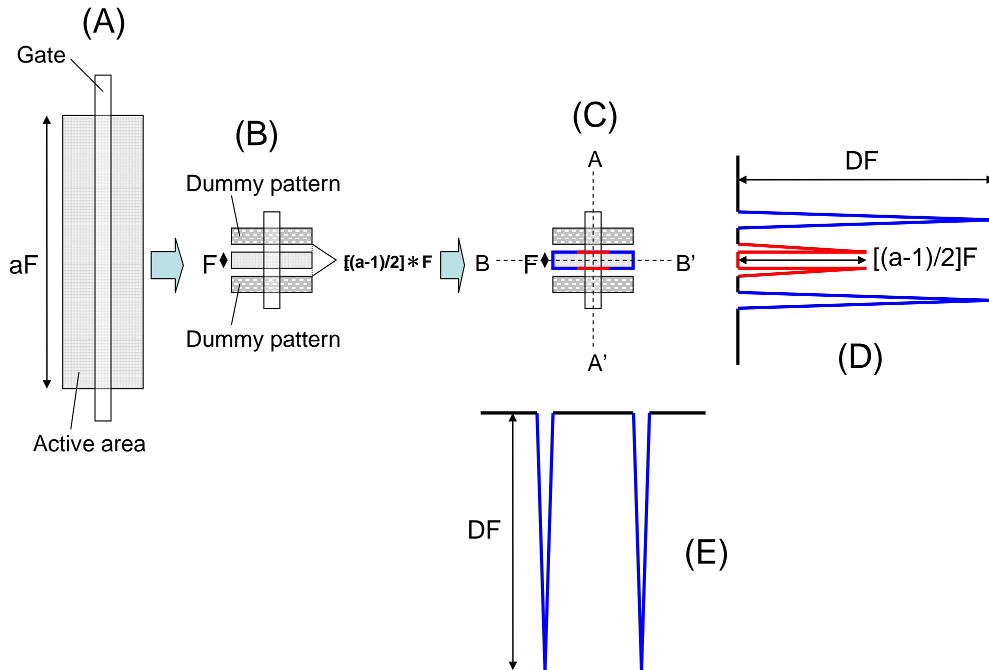
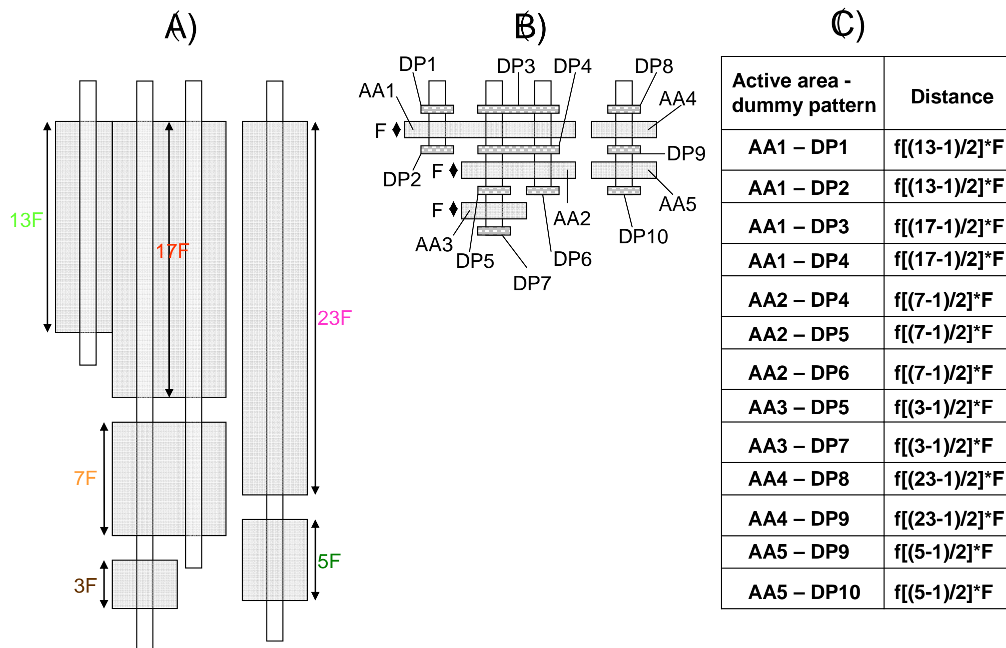



Figure 9: Pattern design of a transistor with simultaneous process, (A)Pattern of planar transistor of channel width aF, (B)Pattern of FinFET with simultaneous process, (C)Top view of FinFET with simultaneous process, (D) AA' cross sectional view of (C), (E) BB' cross sectional view of (C).




| Active area - dummy pattern | Distance |
|---|---|
| AA1 – DP1 | f[(13-1)/2]*F |
| AA1 – DP2 | f[(13-1)/2]*F |
| AA1 – DP3 | f[(17-1)/2]*F |
| AA1 – DP4 | f[(17-1)/2]*F |
| AA2 – DP4 | f[(7-1)/2]*F |
| AA2 – DP5 | f[(7-1)/2]*F |
| AA2 – DP6 | f[(7-1)/2]*F |
| AA3 – DP5 | f[(3-1)/2]*F |
| AA3 – DP7 | f[(3-1)/2]*F |
| AA4 – DP8 | f[(23-1)/2]*F |
| AA4 – DP9 | f[(23-1)/2]*F |
| AA5 – DP9 | f[(5-1)/2]*F |
| AA5 – DP10 | f[(5-1)/2]*F |

Figure 10. Pattern design of circuit with 6 kinds of channel width transistor, (A)Planar pattern, (B) Pattern of circuit with simultaneous process, (C)Distance from active area of FinFET to dummy pattern.

area, sidewall channel width of [(a-1)/2]F can be successfully fabricated as shown in Fig.9 (D). Isolation between the adjacent active area of FInFET is formed by the deep trench isolation of DF. DF is the largest value of trench depth of 50F-100F, as shown in Fig.9 (D),(E).
Next, the design of circuit with 6 kinds of channel width, 3F, 5F, 7F, 13F, 17F, 23F, transistor with simultaneous process has been considered (Fig.10). For realizing 6 kinds of sidewall channel widths, [(3-1)/2]F, [(5-1)/2]F, [(7-1)/2]F, [(13-1)/2]F, [(17-1)/2]F, [(23-1)/2]F simultaneously, 10 dummy patterns, DP1-DP10, are generated in addition to the active area of FinFET, AA1-AA5, ((Fig.10 (B)). The distance from active area for FinFET (AA1-AA5) to dummy patterns (DP1-DP10) are set as shown in Fig.10 (C). Using these dummy patterns, 6 kinds of sidewall channel width (trench depth) can be fabricated simultaneously. The isolation of active area of FinFET of DF is fabricated at the same time. The fabricated pattern with the simultaneous process is shown in Fig.11. Fig.11 (B) shows the BB' cross sectional view. Fig.11 (C) shows the AA' cross sectional view.

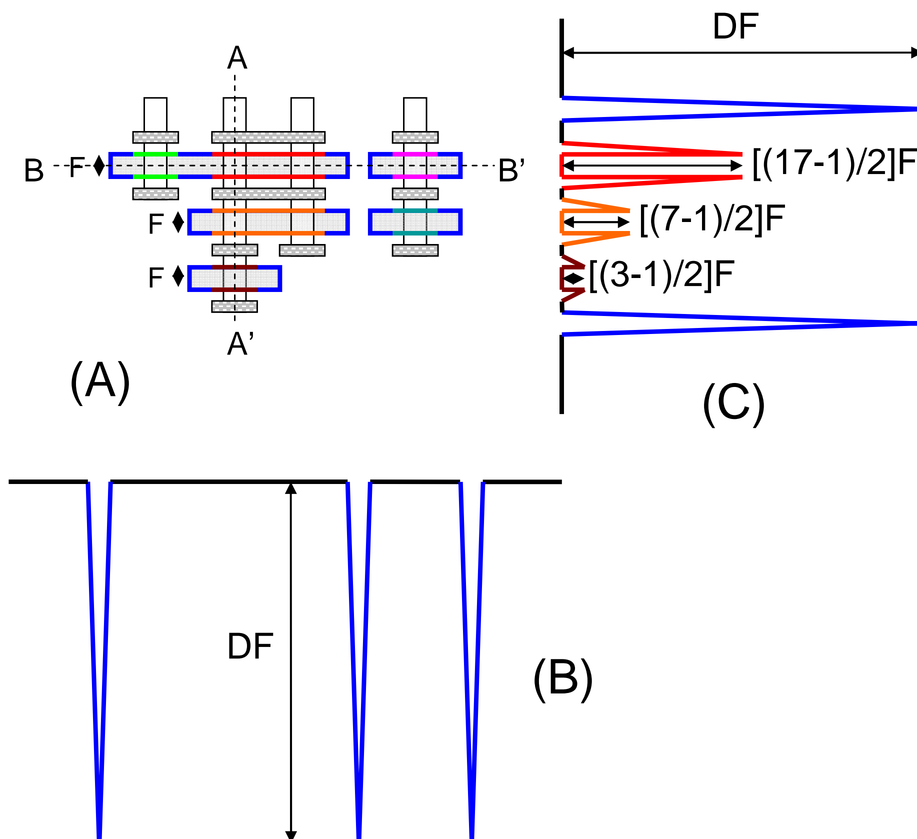



Figure 11. Fabrication pattern of circuit with 6 kinds of channel width transistor, (A)Top view, (B) BB' cross sectional view, (C)AA' cross sectional view.

Reduction of pattern area with simultaneous process is shown in Fig.12. Using this scheme the total channel width which is proportional to the pattern area can be reduced from 92F to 8F. As a result, pattern area can be reduced to 7.6% with only adding one fabrication process of sidewall of simultaneous process (Fig.7 (B)). This reduction of pattern area is also realized with 6 times fabrication of sequential process (Fig.7 (A)). However, this causes the large addition of process steps compared with that of simultaneous process. Therefore, using the simultaneous process, smallest chip cost can be realized compared with that of sequential process as shown in Table 3. This feature is enhanced if the LSI with larger than 100 kinds of channel width is employed.

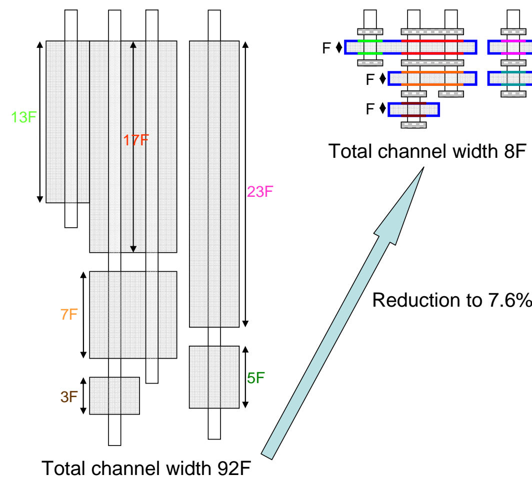



Figure 12: Reduction of pattern area with simultaneous process.

Table 3 Comparison of chip cost of Fig.12 with sequential and simultaneous process assuming that increase in process step is 2%.

| | Pattern area | Addition of process steps | Chip cost |
|---|---|---|---|
| Sequential process | 7.6% | 6 | 7.6*1.12=8.51% |
| Simultaneous process | 7.6% | 1 | 7.6*1.02=7.75% |

And also, by using simultaneous process, LSI can be designed with one kind of pattern except for the dummy pattern of active area independent to the distribution of channel width discussed in section 3. For example, cell libraries of inverter, such as, X1, X2, X4, X8, X16, X32, X64, can be realized with the same pattern

except for the dummy patterns of active area. This enables to reduce the number of masks and pattern design work drastically. This leads to the possibility to change the presently available CAD technology for LSI drastically.

# 5 Conclusion

Study of chip cost of LSI using FinFET with plural number of sidewall channel width is newly described. Using the sequential fabrication of 3-4 kinds of sidewall channel chip cost of buffer circuit and CMOS cell library can be reduced by 5-5.7% compared with of that with conventional single number of sidewall channel width. Further reduction of chip cost can be realized by using simultaneous fabrication process. LSI using FinFET with plural number of sidewall channel width is promising candidate for realizing low cost high density LSI. Furthermore, simultaneous process has the possibility to change the presently available CAD technology for LSI drastically.

## References

[1] International Technology Roadmap of Semicondutor 2003 Edition, 2003 Semiconductor Industry Associatrion.

[2] K. Hieda et. al., "Effect of a new trench-isolated transistor using side wall gates", IEEE Trans. Electron Devices, vol.36, no. 9 , pp.1615-1619, 1989.

[3] D. Hisamoto et. al., "FinFET a self-aligned double gate MOSFET scarable beyond 20nm", IEEE Trans. Electron Devices, vol.47, no.12, pp.2320-2325, 2000.

[4] S. Watanabe, "Design methodology for system LSI with TIS (Trench Isolated-transistor using sidewall gate)", IEICE, vol.J88-C, no.12, pp.1208-1218, 2005.

[5] Intel, Intel 22nm 3-D Tri-Gate Transistor Technology, http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Announcement_Presentation.pdf

[6] S. Davnaraju et. al., "A 22nm IA multi-CPU and GPU system on chip", ISSCC Dig. Tech. Papers, 2012.

[7] Y. Hiroshima and S. Watanabe, "New design technology of independent-gate controlled stacked type 3D transistor for system LSI", IEICE, vol.J92-C, no.3, pp.94-103, 2009.

[8] H. Ishikuro, M. Hamada, K. Agawa, S. Kousai, H. Kobayashi, D. Nguyen, and F. Hatori, "A single-chip CMOS bluetooth transceiver with 1.5MHz IF and direct modulation transmitter,"ISSCC Dig. Tech. Papers pp.68-69, 2003.

[9] S. Watanabe, “New design method of taperd buffer circuit with TIS (Trench - Isolated - transistor using Side wall gate) and its application to high-density DRAMs,” IEICE, vol.J86-C, no.3, pp.301-306, 2003.

[10] D. Heinbuch, “CMOS3 cell library” Addison-Wesley, 1987.

[11] K. Muller et. al, “Trench storage node technology for gigabit DRAM generations”, IEDM Tech Digest, p.507, 1996.

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