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# Design Method of Stacked Type Thermally Assisted MRAM with NAND Structured Cell

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## Abstract

The stacked type thermally assisted MRAM with NAND structured cell which has the features of high speed operation competitive DRAM, non-volatility, and lower bit cost than NAND flash memory has been newly proposed. By using thermally assisted writing scheme, small memory cell size of $5F^2$ and small power consumption during write operation can be realized. Newly proposed scheme with 39nm design rule leads to small chip area of about 70% compared with that of conventional scheme without sacrificing the high speed performance competitive DRAM. Furthermore, write current for memory cell during write operation with newly proposed scheme can be reduced to 1.1% of that of the conventional scheme. This leads to smaller power consumption and smaller chip area and lower bit cost by using the miniaturized design rule such as 22-32nm.

**Keywords**: MRAM, NAND structured cell, spin transistor, thermally assisted writing scheme, BiCS, universal memory

# 1 Introduction

DRAM is widely used for the main memory of personal computer because of its high speed characteristics. On the other hands, NAND flash memory which has the features of non-volatility and low bit cost is widely used for the storage device of the multi-media data. Universal memory which has both features, DRAM and NAND flash memory, is key technology for the future memory system. Recently, the stacked type MRAM with NAND structured cell has been proposed for the candidate of the universal memory [1][2]. By using spin transistor [3] for memory cell, the conventional magnetic writing scheme [4][5][6] generated by a current flow in perpendicular running write bit line and word line can be adopted (Fig.1(A)). However, the scheme has two drawbacks. First is large memory cell size of $9F^2$ (F is design rule) caused by the introduction of write bit line. Second is large write current (power consumption) inherent to the conventional magnetic field writing scheme. This large write current limits the reduction of design rule.
In this paper in order to overcome these drawbacks, stacked type thermally assisted MRAM with NAND structured cell has been newly proposed. This stacked type thermally assisted MRAM use the small heating current of bit line and small current flow of word line for generating magnetic field (Fig.1(B)) as proposed by [7]. The memory cell size of the newly proposed stacked type thermally assisted MRAM can be reduced to $5F^2$, half size of [1], this is because the write bit line for generating magnetic field falls into use. Furthermore, the thermally assisted scheme enables to reduce the writing current of word line and bit line.

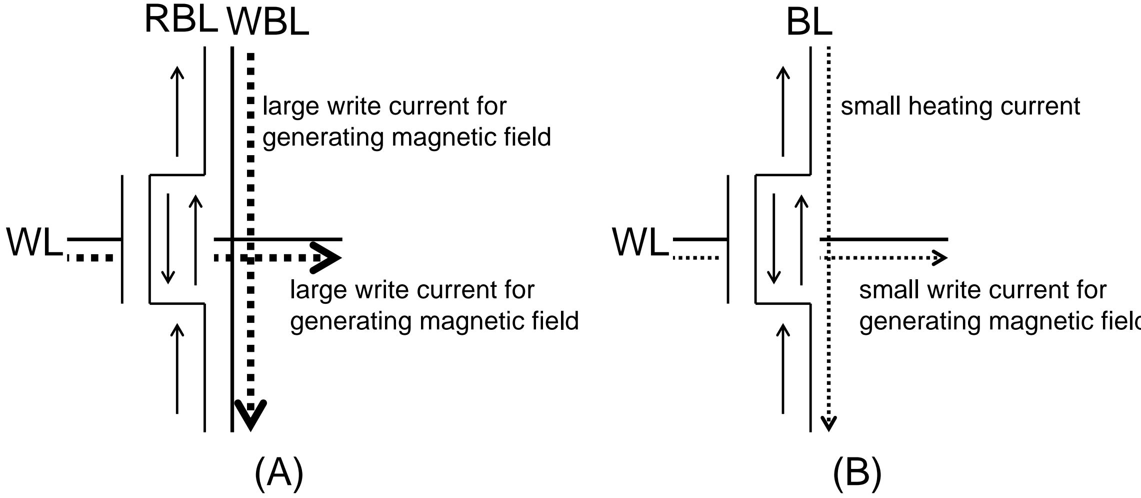



Figure 1 Writing scheme of the conventional MRAM [1] and newly proposed MRAM, (A)conventional MRAM, (B) proposed MRAM

This paper is organized as follows. Section 2 describes the cell structure of newly proposed stacked type thermally assisted MRAM with NAND structured cell. Section 3 presents the read and write operation of newly proposed thermally assisted MRAM. Section 4 describes the design of core circuit such as row decoder and estimation of the pattern area. Finally, a conclusion of this work is provided in Section 5.

# 2 Cell structure of stacked type thermally assisted MRAM

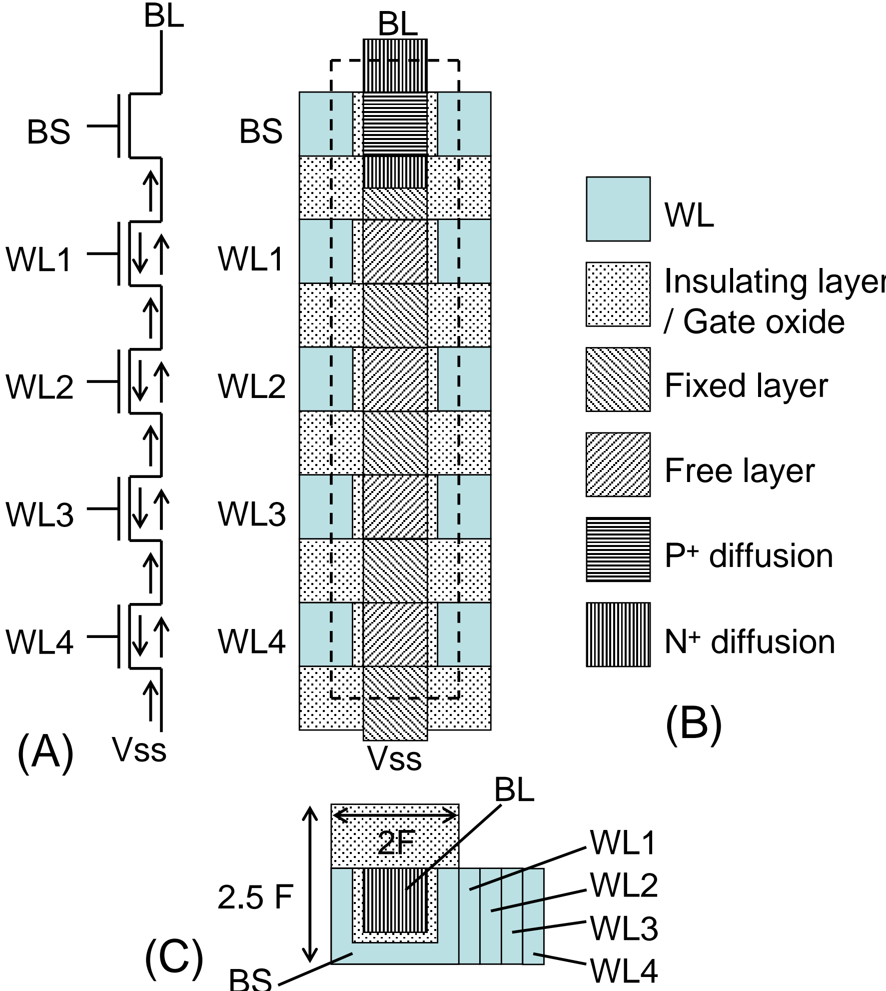



Figure 2: Configuration of newly proposed memory cell (A)Equivalent circuit, (B)Cross-sectional view (C) Top view

The cell structure of newly proposed stacked type thermally assisted MRAM is

shown in Fig.2. The cell structure of conventional stacked type MRAM is shown in Fig.3 for comparison. As shown in Fig.2 (A) there is no write bit line (WBL) which is inherent to the conventional stacked type MRAM (Fig.3 (A)).

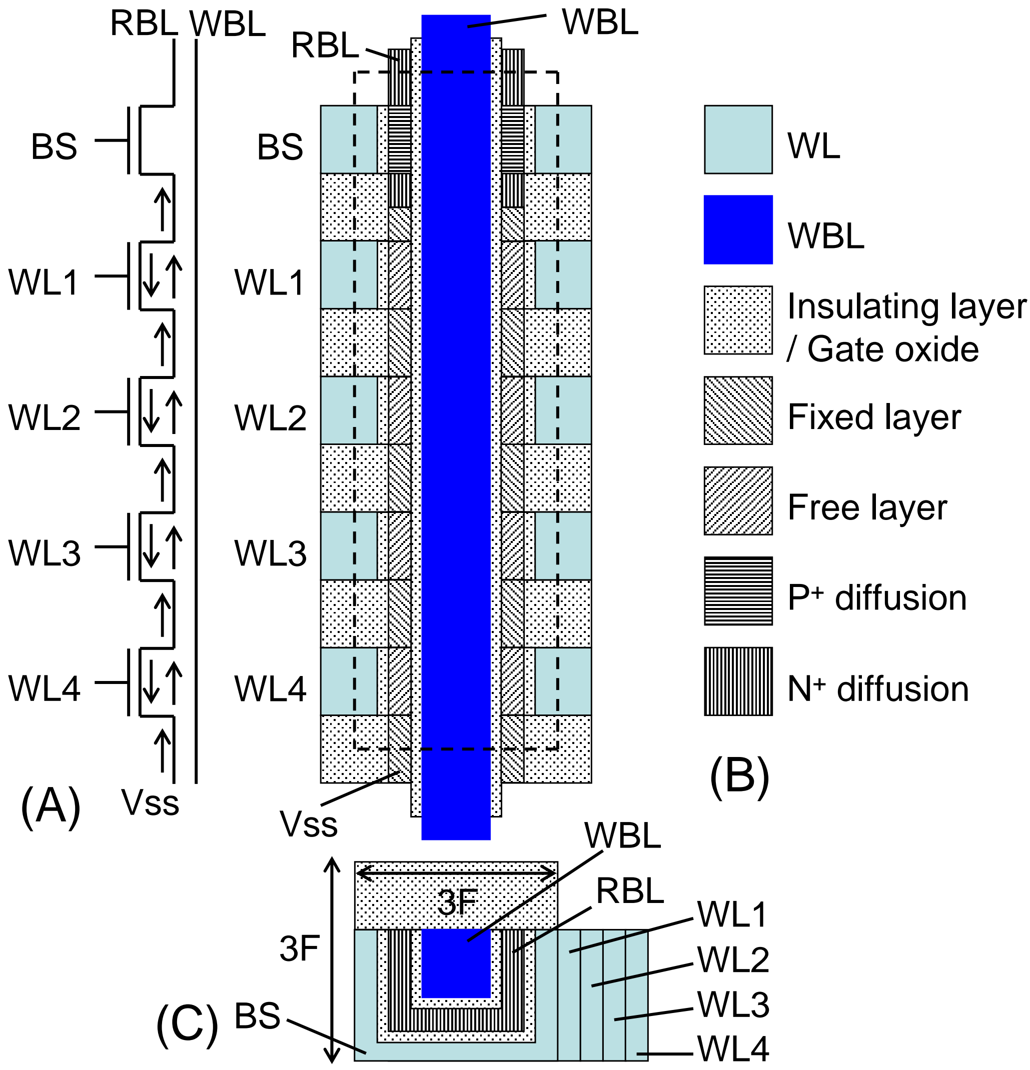



Figure 3: Configuration of conventional memory cell (A)Equivalent circuit, (B)Cross-sectional view (C) Top view

This leads to the reduction of memory cell size from $3F*3F=9F^2$ (Fig.3 (C)) to $2.5F*2F=5F^2$ (Fig.2 (C)). Furthermore, the simple structure of the cross sectional view of memory cell (Fig.2 (B)) compared with that of (Fig.3 (B)) enables to reduce the number of process steps. BiCS structure is adopted [8][9]. Both small cell size of $5F^2$ and small number of process steps results in the lower bit cost. However, in the case of newly proposed scheme for writing digital value of “0” or

"1" the bi-directional write current scheme should be introduced to WL. This leads to double ended arrangement of the row decoder which occupies large pattern area. Therefore, the optimized cell array design of the newly proposed thermally assisted MRAM is the key issue for realizing low bit cost.

# 3 Read and write operation of newly proposed scheme

## 3.1 Design of WL

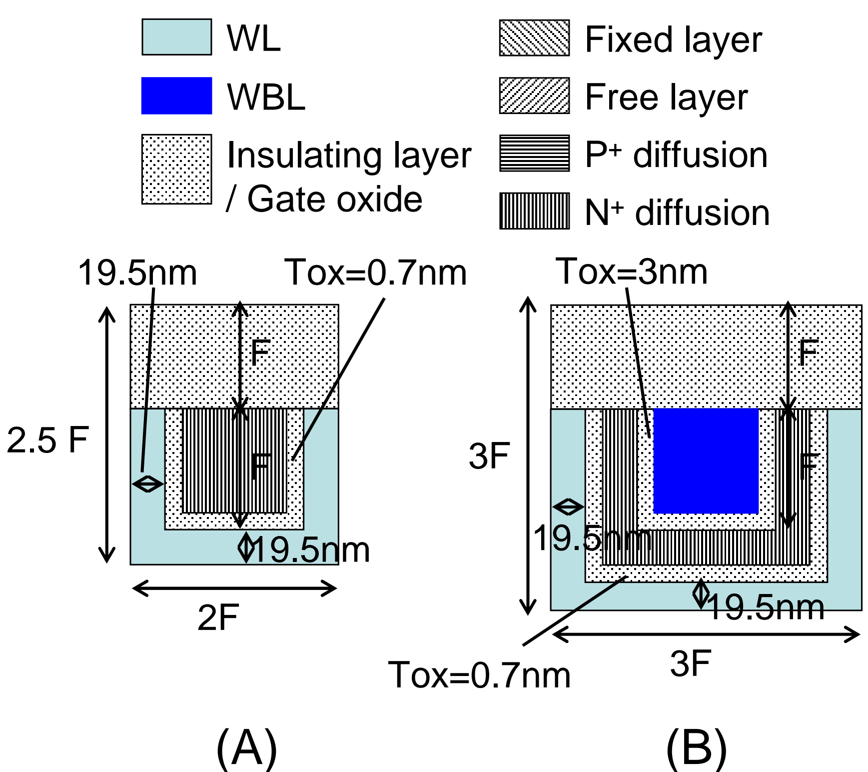
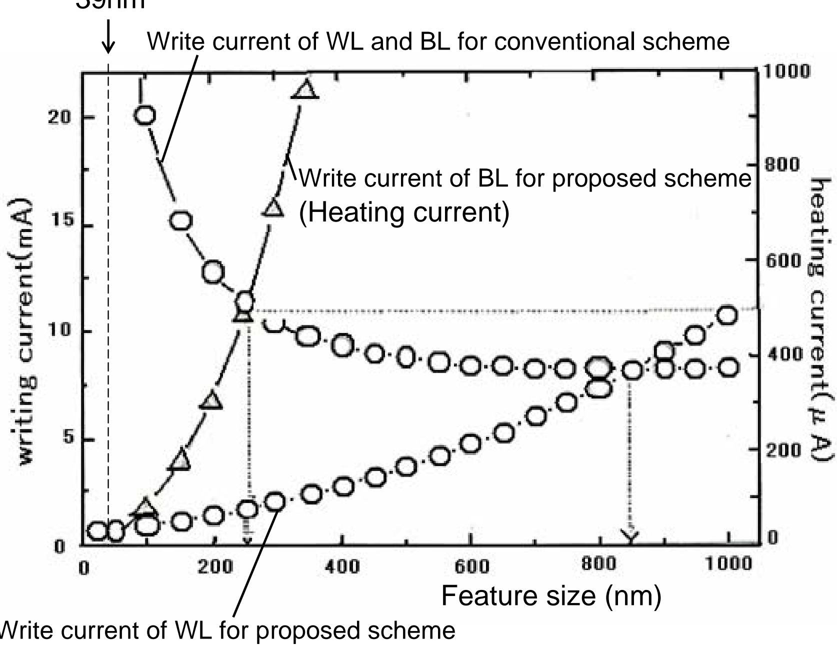



Figure 4: Top view of memory cell (A) Newly proposed scheme, (B) Conventional scheme

As described in section 1, the target specification of the newly proposed stacked type thermally assisted MRAM are high speed operation competitive DRAM, non-volatility, and lower bit cost than NAND flash memory. To realize high speed operation competitive DRAM, delay time of WL and delay time of BL should be limited to smaller than 10% of DRAM access time of 50ns (5ns)[1].
For the optimization of cell array structure of newly proposed scheme the resistance and capacitance of WL are estimated using the top view and cross-sectional view of memory cell. These values are compared with that of the conventional scheme. The top view of memory cell is shown in Fig.4 ((A)Newly

proposed scheme, (B)Conventional scheme).
The resistance of WL per cell is 0.267Ω using the pattern of WL shown in Fig.4 (A) and sheet resistance of 0.1Ω. This value is 59% of that of conventional scheme (Fig.4 (B)). This reduction of the resistance is caused by the reduction of memory cell size parallel to WL running direction ( from 3F to 2F ). On the other hands, the WL capacitance per cell is 0.27fF which is 60% of that of conventional scheme (Fig.4 (B)). This reduction of the capacitance is caused by the reduction of channel width ( from 5F to 3F ) due to reduction of memory cell size ( from $9F^2$ to $5F^2$). As a result the delay time of WL which can be estimated 1.11pF* 1.09KΩ becomes 1.21ns, if 4K memory cells which is the same value as the conventional scheme are connected to one WL. This delay time is as small as 43% of that of the conventional scheme. Therefore, 4K*2=8K memory cells can be connected to one WL without sacrificing the upper limit of the WL delay time of 5ns. In this paper for realizing lower bit cost than NAND flash memory small chip size is key issue. It is assumed that 8K memory cells are connected to one WL for reducing the pattern area of row decoder. Further discussion is described in the next section.

## 3.2 Design of write and read current of memory cell




The Figure 5: Write current of WL and BL vs. feature size F

The feature of the thermally assisted MRAM is the drastical reduction of write current compared with the conventional magnetic writing scheme. The write current vs. feature size F is shown in Fig.5[7]. For the conventional magnetic writing scheme, write current for WL and BL increases as decreasing the feature

size. As a results, in the case of 39nm the write current for WL and BL become larger than 20mA. This causes large power consumption and the degradation of the reliability for the wiring. For the other hands, for the thermally assisted MRAM case, write current for WL and BL decreases as decreasing the feature size. This results in small write current of 0.5 mA for WL, and 40uA (heating current) for BL in 39nm case. This leads to the reduction of design rule. For the read operation read current, IR, of 10uA is also adopted. In the later section these values are used for the design of core circuit of the thermally assisted MRAM.

## 3.3 Read disturb and write failure caused by charging current of WL

In the ref [7] the charging of the selected WL and discharging of the selected BL for sensing the memory cell data or warming the selected memory cell up is performed simultaneously. However, in newly proposed stacked type thermally assisted MRAM (newly proposed scheme) case, this procedure results in read disturb and write failure as shown in Fig.6.

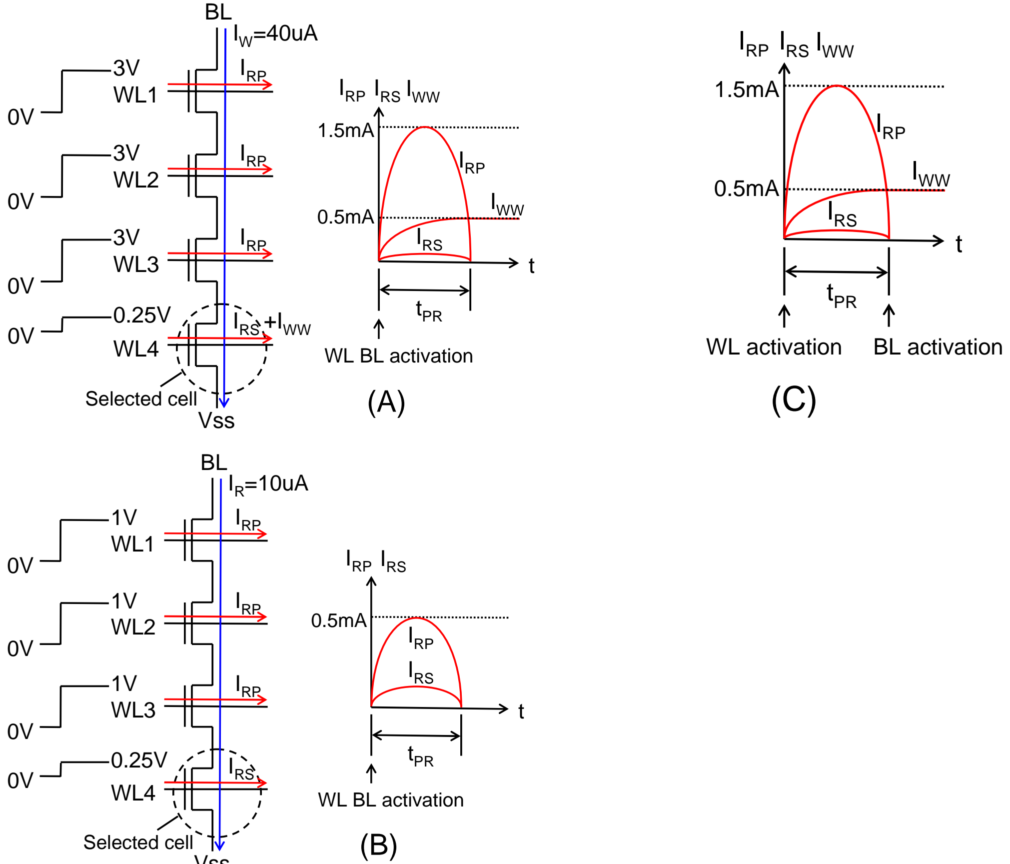



Figure 6: (A) write failure with WL, BL activation simultaneously, (B) read disturb with WL , BL activation simultaneously, (C) New technique of BL activation after charging process of WLs.

In the newly proposed scheme write operation is performed with constant current flow along selected WL (WL4) of 0.5mA and current flow along selected BL of 40uA. In this case the AC current flows along the pass WLs (WL1, WL2, WL3) for charging the pass WLs about 4ns (delay time of WL) as shown in Fig.6 (A). The value of this charging AC current is 2.2pF*3V/4ns=1.5mA. This value is larger than that of constant DC current of 0.5mA for the write operation. As a result, the passed memory cells connected to WL1, WL2, WL3 suffered from write failure due to the current flow along selected BL of 40uA for warming the selected memory cell up.
The same problem will be occur during read operation (Fig.6 (B)). In the newly proposed scheme read operation is performed with current flow along selected BL of 10uA. Furthermore, the AC current of 0.5mA (=2.2pF*1V/4ns=0.5mA) flows along the selected and pass WLs (WL1, WL2, WL3,WL4) for charging the WLs about 4ns. As a result read disturb problem occurs to the passed and selected memory cells connected to WL1, WL2, WL3, WL4.
In order to overcome these write failure and read disturb problems in the newly proposed scheme the technique of BL activation after charging process of WLs has been adopted (Fig.6 (C)). Using this technique the write failure and read disturb problems can be drastically reduced.

## 3.4 Read and write operation

Read operation of newly proposed stacked type thermally assisted MRAM is shown in Fig.7. For realizing the write operation the double ended row decoder scheme has been introduced for the bi-directional current flow along the selected WL. Three NAND structures located in the left edge, right edge and the center of the memory cell array is shown in Fig.7. It is assumed that the data of memory cell connected to WL4 is read out to BL N/2 (N=8K). Read operation is almost the same as that of ref[1] of the conventional magnetic writing scheme except for the technique of BL activation after charging process of WLs. For avoiding the mal-function inherent to the NAND structure [1][2] large resistance of the selected cell and small resistance of the passed cell must be achieved simultaneously. For realizing small resistance of the passed cell large voltage of 1V ( threshold voltage VT=0.2V) is applied to the WLs (WL1, WL2, WL3). And also, for realizing large resistance of the selected cell small votage of 0.25V (VT=0.2V) is applied to the selected WL (WL4). After these activation and the charging process of WLs, BL N/2 is activated to read out the memory cell data. For the high speed operation large read current, IR, is desiable. However, larger read current results in the read disturb of the selected cell. Therefore, for avoiding this read disturb IR=10uA which is 1/4 of write current (IW=40uA) is adopted. Further discussion about IR is described in section 3.6. During read operation the unselected BLs are set to 0V.

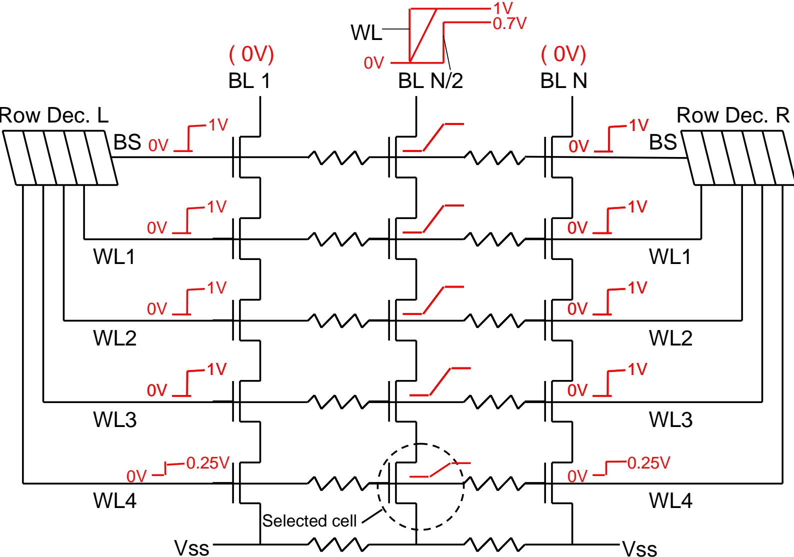



Figure 7: Read operation of newly proposed scheme

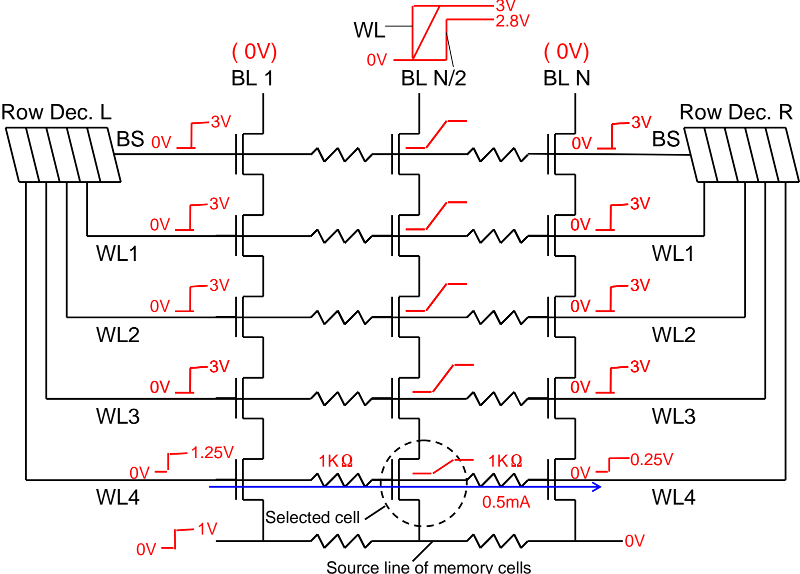



Figure 8: Write operation of newly proposed scheme

Write operation of newly proposed stacked type thermally assisted MRAM is shown in Fig.8. Three NAND structures located in the left edge, right edge and the center of the memory cell array is shown in Fig.8. It is assumed that for writing the data to selected cell the current flows from left to right direction along the selected WL (WL4). Write operation of the newly proposed scheme is different from that of ref[1] of the conventional magnetic writing scheme. In the newly proposed scheme write current, IW, of 40uA flows from the selected

BL N/2 to source for warming the selected cell up. For avoiding the write failure of the passed cell during write operation the resistance of the passed cell must be small. For this purpose large voltage of 3V is applied to the WLs (WL1, WL2, WL3). For realizing the stable operation of the selected cell large resistance of the selected cell should be realized for warming the selected cell sufficiently up. For this purpose slightly larger voltage than VT=0.2V, 0.25V, is applied to the selected WL (WL4).

Furthermore for realizing the current flow of 0.5mA from left to right direction the output voltage of left side row decoder is set to 0.25V+0.5mA*2KΩ=1.25V and of right side row decoder is set to 0.25V. And also, for realizing the constant resistance of selected cell independent to the position within the memory cell array new design scheme with the source line of cells has been introduced. As shown in Fig.8 the source electrode of cells which is connected to WL4 is connected along WL running direction (the source line of cells). During write operation the voltage of left edge of the source line of cells is set to 1V and the voltage of right edge of the source line of cells is set to 0V. With this procedure the voltage of selected cell (VG-VT-VS) becomes constant value of 0.25V-0.2V=0.05V independent to the position within the memory cell array. As a result, the constant resistance of selected cell independent to the position within the memory cell array can be realized. During write operation the unselected BLs are set to 0V.

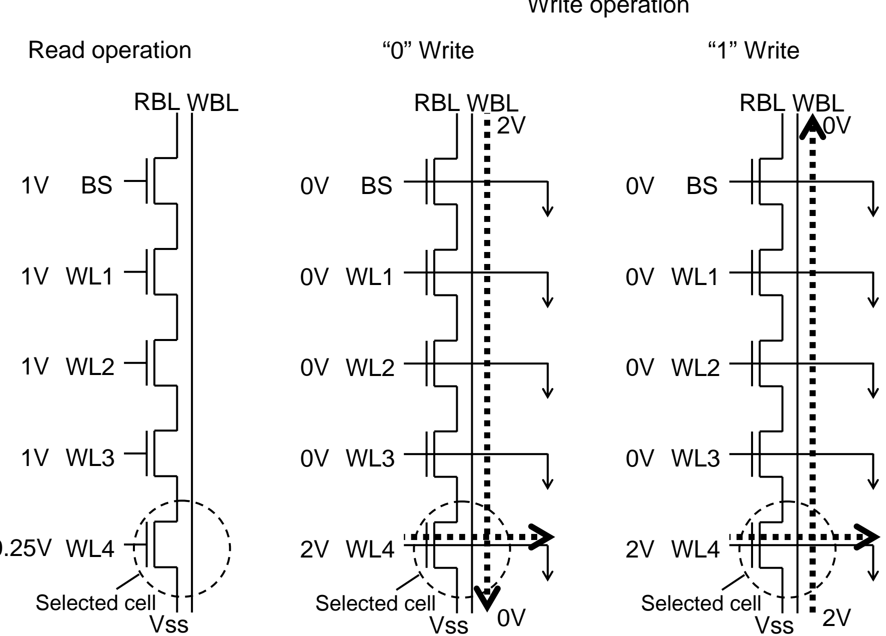



Figure 9: Read and write operation of conventional magnetic writing scheme

Read and write operation of conventional magnetic writing scheme[1] is shown in Fig.9 for comparison.

## 3.5 Estimation of write failure to adjacent memory cells

In section 3.3 and 3.4 read disturb and write failure due to the charging current of WL can be overcome by using the technique of BL activation after charging process of WLs and the constant resistance of selected cell technique using the source line of memory cells. The residual problem for stable read and write operation is write failure to the adjacent memory cells caused by the magnetic leakage field and leak of heat from the selected memory cell. This problem is discussed in this section.
The magnetic leakage field is shown in Fig.10. The magnetic field is proportional to current of selected WL , $I_{WW}$, and is inversely proportional to the distance from selected WL. The distance from the selected WL to the channel region of the selected memory cell is 0-0.5F assuming that the thickness of gate dielectric is negligibly small. The average value is 0.25F. The distance from the selected WL to the channel region of the adjacent memory cell is F-3F. The average value is 2F. Therefore, the value of magnetic leakage field of the adjacent cell is 0.25F/2F=0.125 of that of the selected cell. As a result this small magnetic leakage field will not cause the write failure to the adjacent cells.

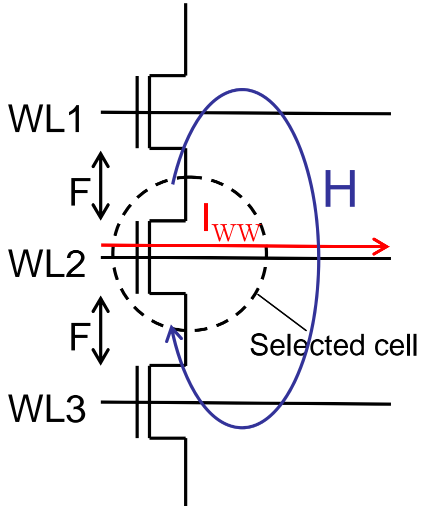



Figure 10: Write failure caused by magnetic leakage field.

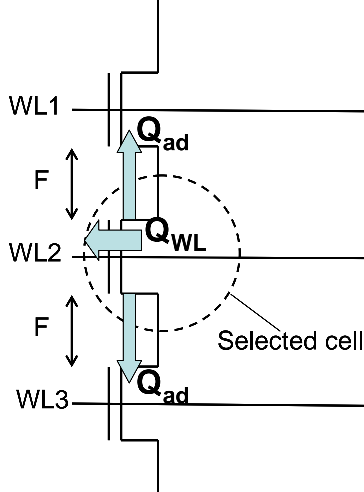



Figure 11: Write failure caused by leak of heat.

The leak of heat is shown in Fig.11. There are three leak paths of heat, to two adjacent cells and to selected WL. These leaks are represented by heat flow Qad and $Q_{WL}$ as shown in Fig.11. The heat flow is proportional to difference in temperature and is inversely proportional to the thermal resistance[10]. The thermal resistance is proportional to the length and inversely proportional to the cross section and the thermal conductivity. As for the leak to the adjacent cell length is F and cross section is $F^2$. As for the leak to the selected WL length is 0.02F and cross section is $3F^2$. The thermal conductivity of Si for the adjacent

memory cell is about 170 times larger than that of $SiO_2$ for the selected cell. Using these value the thermal resistance of leak to the adjacent cell and to the selected WL become almost the same value. Therefore, heat flow to the adjacent cell and to the selected WL become almost the same value ($Qad = Q_{WL}$) assuming that the temperature of the selected WL and the channel region of the adjacent cell is equal. As a result the generated heat within the selected cell is divided equally among three. Because the value of magnetic leakage field of the adjacent cell is as small as 0.125 of that of the selected cell, this leak of heat to the adjacent cell will not cause the write failure to the adjacent cells.

## 3.6 Design of BL

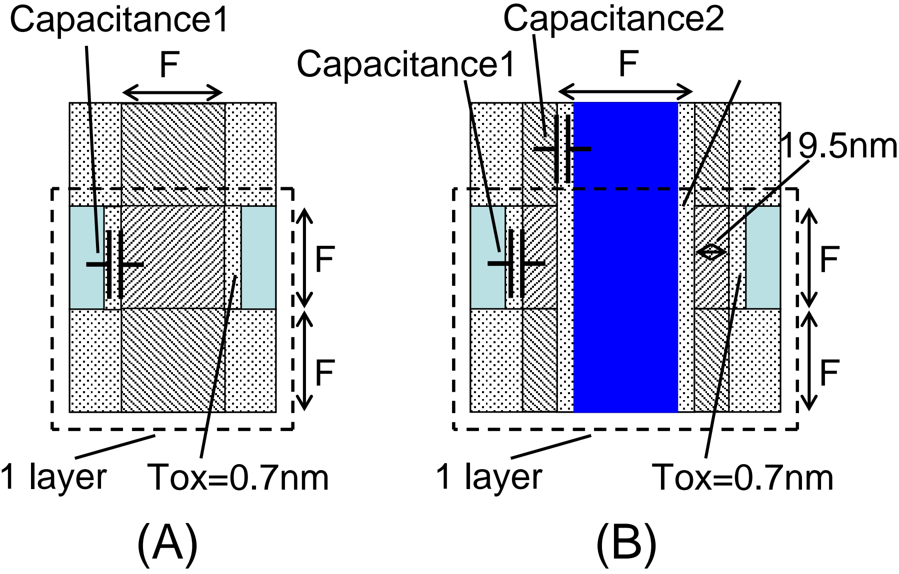



Figure 12: Cross-sectional view of memory cell (A) Newly proposed scheme, (B) Conventional scheme

For realizing high speed operation competitive DRAM delay time of BL should be limited to smaller than 10% of DRAM access time of 50ns (5ns)[1].

For estimating the delay time of BL, the capacitance and the resistance of BL are calculated using cross-sectional view of memory cell (Fig.12 (A)) and compared with that of the conventional scheme (Fig.12 (B)). The capacitance of BL per cell ( per stage ) is 0.27fF which is consisted with Capacitance1. This value is 56% of that of conventional scheme, because there is not Capacitance2 as shown in Fig. 5 (A). The resistance of BL is estimated using the equivalent resistance of the spin transistor [1][2]. The resistance of selected spin transistor is 35KΩ which is 66.7% larger than that of the conventional scheme case. For this estimation gate length of 39nm, channel width of 117nm and gate oxide thickness of 0.7nm is adopted. This increase in the resistance is caused by the reduction of channel width ( from 5F to 3F ). Therefore, the resistance of BL which equals to (the

resistance the selected spin transistor) + (the total resistance of passed spin transistors) is 35K Ω+35K Ω=70K Ω. This value is independent of the number of stages of stacked cell[1][2]. As a results, the delay time of BL becomes 0.017pF*70K Ω=1.21ns, if 64 stage which is the same value as the conventional scheme is introduced. This value is as almost the same value as the conventional scheme, because the increase in resistance is compensated with the reduction of capacitance. Therefore, 64 stages can be introduced without sacrificing the upper limit of the BL delay time of 5ns.
For realizing the read operation read current of 10uA (IR=10uA) should be adopted to the selected BL as described in section 3.2 and 3.4. Therefore, the voltage of the selected BL during read operation should be applied to 70KΩ *0.01mA=0.7V. The voltage of WL for the passed transistor is set to 0.7V+VT=0.7V+0.2V=0.9V≒1.0V for read operation. For realizing the write operation write current of 40uA (IW=40uA) should be adopted to the selected BL as described in section 3.2 and 3.4. Therefore, the voltage of the selected BL during read operation should be applied to 70KΩ*0.04mA=2.8V. The voltage of WL for the passed transistor is set to 2.8V+VT=2.8V+0.2V=3V for write operation. These procedures of designing the BL for read and write operation is shown in Fig.13.

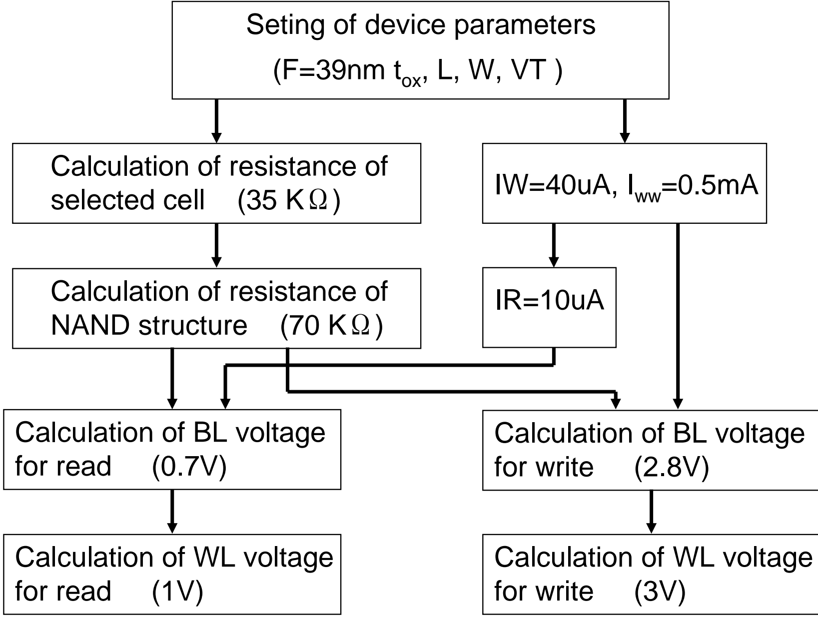



Figure 13: Procedures of designing the BL for read and write operation

# 4 Design of core circuit

## 4.1 Configuration of core circuit including memory cell array

The configuration of the newly proposed stacked type thermally assisted MRAM is shown in Fig.14. Four memory cells are connected in series for simplicity. The main features of this scheme compared with conventional magnetic field writing scheme [1] is as follows.

(1) In the newly proposed scheme the double ended row decoder arrangement is required for bi-directional write current scheme for WL. As a result, the pitch (width) of row decoder must be designed within 2.5F which is equal to the length of memory cell (Fig.2).
(2) In the newly proposed scheme source electrode of WL4 (Fig.14) is connected along the WL running direction. Both side of the source line of memory cells is set to 0.25V(left edge)/1.25V(right edge) or 1.25V(left edge)/0.25V(right edge) during write operation.

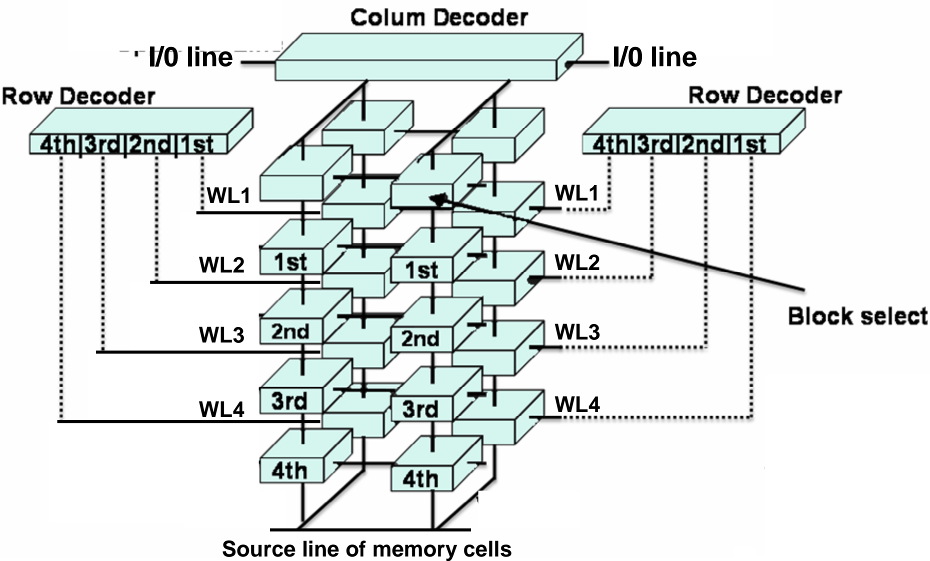



Figure 14: Configuration of the newly proposed stacked type thermally assisted MRAM

## 4.2 Design of row decoder circuit

Row decoder circuit is shown in Fig.15. It is assumed that WL4 is selected. Circuit itself is almost the same as the conventional magnetic field writing scheme

[1]. For realizing bi-directional write current scheme of selected WL during write operation the driving signal of the selected WL $V_{LOWL}$ for the left hand side row decoder and $V_{LOWR}$ for the right hand side row decoder are adopted. Row decoder drive circuit is shown in Fig.16. Newly introduced $V_{LOWL}$ and $V_{LOWR}$ are generated using the row decoder drive circuit.

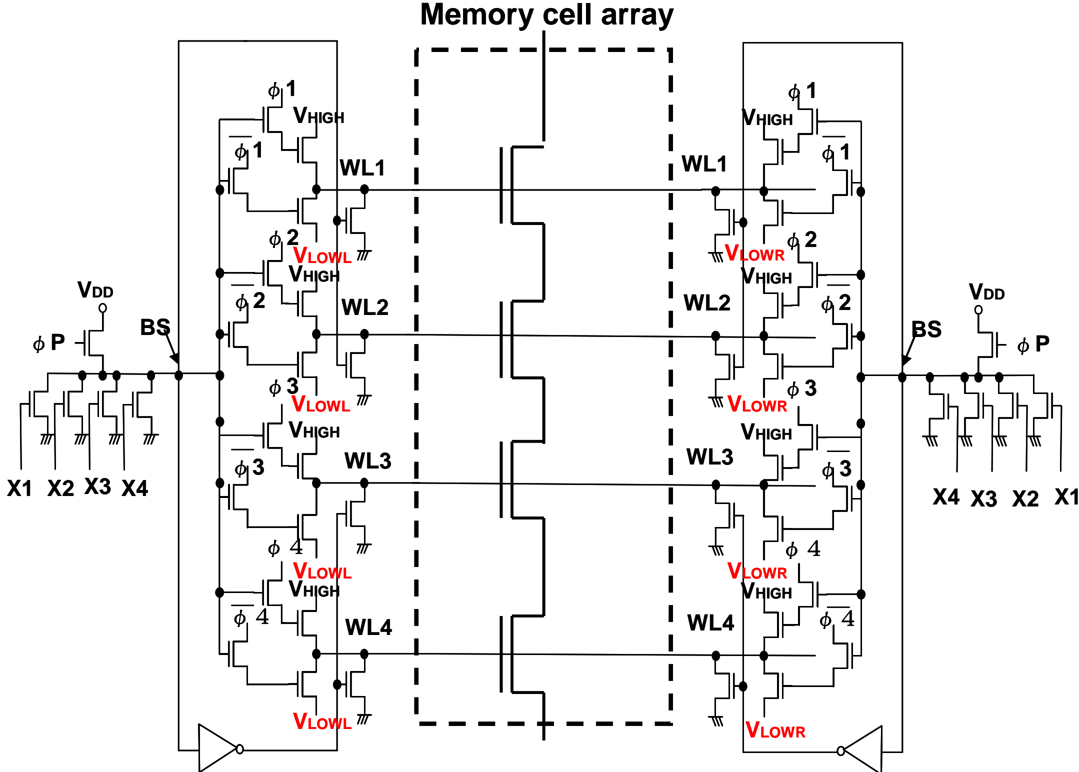



Figure 15: Row decoder circuit

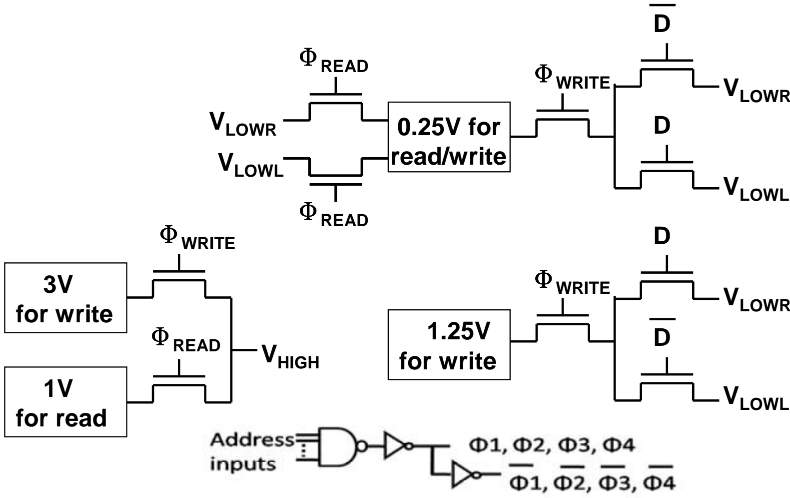



Figure 16: Row decoder drive circuit

Top view and cross sectional view of row decoder pattern for the newly proposed scheme is shown in Fig.17. For realizing small pattern area SGT [12][13] has been adopted. The pattern is almost the same as the conventional magnetic writing scheme. This is because almost the same circuit is used for the newly proposed scheme. For reducing the pitch (width) of row decoder from 3F of conventional scheme to 2.5F, the design rule about the alignment is miniaturized compared with that of conventional scheme. The length of row decoder for the WL dunning direction is 1865F which is the same value as the conventional scheme.

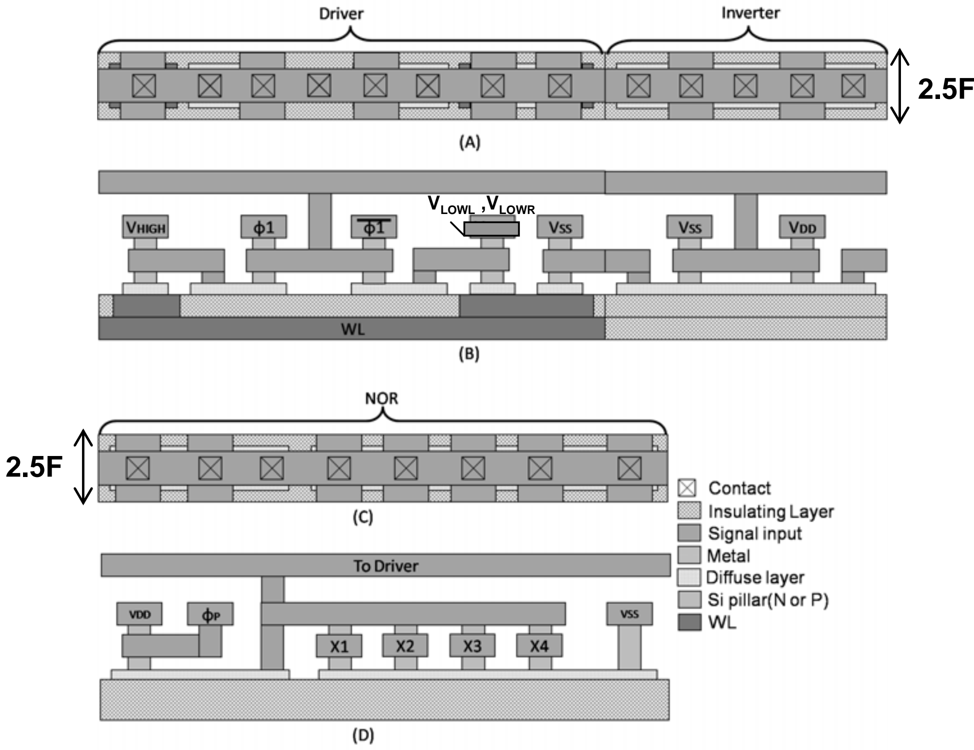
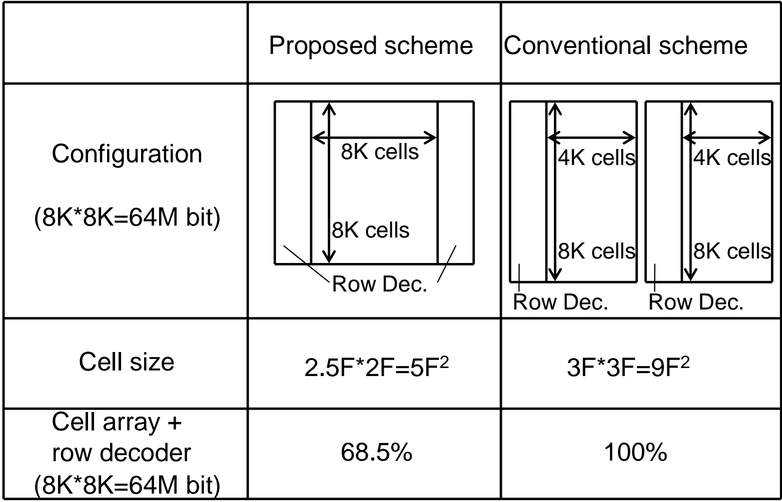



Figure 17: Row decoder's SGT pattern
(A) Top view of driver and inverter's layout
(B)Cross-sectional view of driver and inverter's layout
(C) Top view of NOR's layout
(D)Cross-sectional view of NOR's layout

## 4.3 Estimation of pattern area of core circuit

The pattern area of the core circuit , memory cell array and row decoder, is shown in Fig.18. It is assumed that the size of memory cell array is 8K*8K=64M bit for 1 layer. As described in section 2 the memory cell size, memory cell area for 1 bit, of the newly proposed scheme is reduced to 55.6% compared with that of the

conventional magnetic field writing scheme. Furthermore, due to the reduction of resistance and capacitance for memory cell 8K memory cells which is twice as large as the conventional scheme can be connected to one WL without sacrificing the performance. This leads to the reduction of the number of row decoder. As a result, the pattern area of core circuit can be reduced to 68.5% of that of the conventional magnetic field writing scheme. The almost chip area is occupied by the core circuit (85-90%)[14]. Therefore, the chip area with newly proposed scheme can be reduced to about 70% of that of the conventional scheme.



| | Proposed scheme | Conventional scheme |
|---|---|---|
| Configuration (8K*8K=64M bit) | 8K cells, 8K cells, Row Dec. | 4K cells, 8K cells, Row Dec.; 4K cells, 8K cells, Row Dec. |
| Cell size | 2.5F*2F=5F$^2$ | 3F*3F=9F$^2$ |
| Cell array + row decoder (8K*8K=64M bit) | 68.5% | 100% |

Figure 18: The pattern area of the core circuit , 64Mbit memory cell array and row decoder

# 5 Conclusion

| | Proposed scheme | Conventional scheme |
|---|---|---|
| Cell current (F=39nm) | $I_W$=0.5mA<br>$I_{BL}$=0.04mA<br>$I_W+I_{BL}$=0.54mA | $I_W$=25mA<br>$I_{BL}$=25mA<br>$I_W+I_{BL}$=50mA |
| | 1.1% | |
| Chip area | 70% | 100% |
| Access time | 1 | 1 |

Figure 19: The feature of newly proposed scheme

The features of the newly proposed stacked type thermally assisted MRAM for F=39nm is summarized in Fig.19. By using the newly proposed scheme, small cell size of 5F$^2$ can be realized. This leads to small chip area of about 70% compared with that of the conventional scheme without sacrificing the high speed

performance competitive DRAM. Furthermore, write current for memory cell during write operation with newly proposed scheme can be reduced to 1.1% of that of the conventional scheme. This leads to smaller power consumption and smaller chip area and lower bit cost by using the miniaturized design rule such as 22-32nm. The newly proposed scheme is the promising candidate for realizing high-speed and low bit cost non-volatile semiconductor memory.

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