Contemporary Engineering Sciences, Vol. 2, 2009, no. 4, 149 - 163

A Novel Five-Input Configurable Cell Based on Irreversible Single Electron Box

Naeimeh Soheili

Islamic Azad University, Science and Research Branch, Tehran, Iran.
soheili@ieee.org

Davoud Bahrepour

Islamic Azad University, Science and Research Branch, Tehran, Iran.
bahrepour@ieee.org

Payman Loloeyan

p_loloeyan@ieee.org

Keivan Navi

Faculty of Electrical and Computer Engineering
Shahid Beheshti University, Tehran, Iran
navi@sbu.ac.ir

Abstract

This paper proposes two configurable cells designed using irreversible single electron box (SEB). Each cell consists of two SEB that serially connected to each other. Each SEB acts as a complementary majority gate and comprises a capacitor array for applying inputs and an irreversible single electron box in order to producing the output. By applying appropriate input logic to the control gate(s), the cells act as majority, buffer, AND and OR logic gates. The proposed configurable cells enable us for designing low-power LSI chips which are suitable for different usage such as mobile applications. As an application, a full adder based on proposed cell is designed. All the simulations for proposed cell have been performed with a Monte-Carlo based simulator, called SIMON.

Keywords: Configurable cell, irreversible single electron box, full adder, majority gate

1 Introduction

Current technologies like CMOS will encounter with technological limitations shortly after 2010 [14]. Rapid movement into nanoscale devices needs structures that overcome the technological problems, however, present small size devices. Single electron devices which use coulomb blocked effect [7], are one of the promising candidates for nanoelectronic applications. Single electron circuit works by controlling one-by-one electron transfer [3], hence the device size and power dissipation decrease drastically. These characteristics render small size circuits with ultra low power consumption. Already, lots of single electron based circuits are introduced in literatures such as memories [6], majority gate [4], analog to digital converter [1], and saturating counter [8].

In this paper, first, a two input and a three input single electron based configurable cells are introduced which by different configurations of these cells, buffer, majority, AND and OR functions can be gained. Then using these two cells, two full adders are introduced. Proposed full adders are simulated using SIMON simulator [13] which is a Monte-Carlo based simulator for single electron circuits and provides common tunneling. Also, the comparisons of full adders are presented. The paper continues as follows:

In Section 2, a majority gate is introduced and in Section 3 a three-input configurable cell based on single electron box is explained and configured to generate some logic gates. A novel five-input configurable cell based on single electron box introduced in Section 4 and in Section 5, this novel cell is configured in order to design some logic gates. By exploiting introduced cells two Full Adders are designed and presented in section 6 and the comparison of these two Full Adders and related simulation results are reported. Conclusions follow in section 7.

2 Majority Gate Using Irreversible Single Electron Box

The main component of the proposed cell is an irreversible single electron box comprises a double tunneling junction. A tunnel junction consists of two pieces of metal separated by a very thin (~10 nm) insulator. Electrons are able to travel from one of the metal electrode to the other metal electrode by tunneling through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction flows in multiples of *e*, the charge of a single electron. Fig.1 (a) shows an irreversible single electron box with a double tunnel junction. It comprises two identical tunneling junctions $Cj = 20aF$, a bias capacitor $C_L = 2aF$ and a bias voltage V_d. It has an island node "1" at which electrons is stored [4].

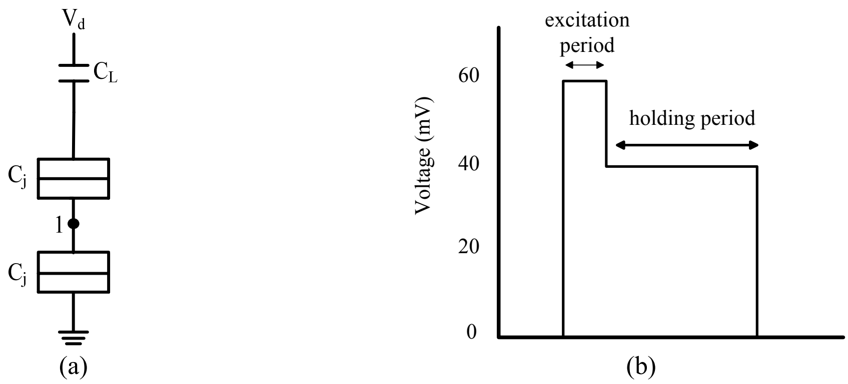


Fig.1.(a) An irreversible single electron box (SEB) with a double tunnel junction [6].(b) a two-step pulse that shows excitation and holding period (selected from [4]).

T. Oya, *et al.* introduced a majority device using irreversible single electron box [6]. As shown in Fig.2 (a) the proposed structure consists of a capacitor array (C) and an irreversible single electron box. Input voltages V_1, V_2 and V_3 are applied to node 2 through input capacitors. The input voltages V_1, V_2 and V_3 should be 4mV or -4mV for representing logic '1' or '0'. The irreversible single electron box then produces the complementary majority logic output on node 2. The bias voltage V_d in complementary majority logic is a two-step clock pulse which is 60 mV (excitation voltage) and then is set to 40 mV (holding voltage) (Fig. 1(b)). Inputs which are rectangular pulses are applied to the capacitor array for input summation during excitation voltage and then are set to 0 V through holding voltage. The output is produced during holding voltage.

3 A Three-Input Configurable Cell Based on SEB

Fig. 2(a) illustrates a SEB that acts as a complementary majority gate. In this section a configurable cell based on irreversible single electron box is introduced comprises of two serially connected SEBs [2]. Fig.2 (b) depicts proposed three-input cell. By applying different values to the inputs V_1, V_2 and V_3, the cell will produce different logic as output, while C_1 and C_2 are logic 1 and 0 respectively.

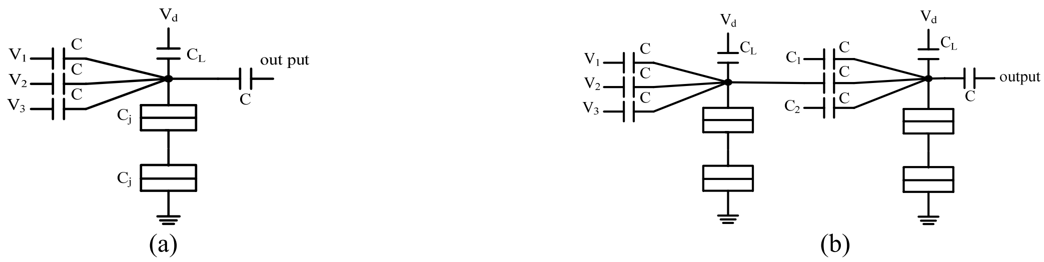


Fig.2.(a) a complementary majority gate based on irreversible single electron box [6].(b) a novel three-input cell for producing different logic by applying appropriate voltage (logic levels) to the inputs.

3-1 A Three-Input Majority Gate

By the use of majority logic, digital operation can be done. A majority gate is a voter. It receives odd number of inputs and produces an output. The output is a logical 1 when the majority of inputs are logical 1 and a logical 0 when the majority of inputs are logical 0. A three-input majority function can be expressed in terms of fundamental boolean operators as Eq. 1:

$$M(a,b,c) = ab + ac + bc \quad (1)$$

A complementary majority gate produces logical 1 when the majority of inputs are logical 0 and a logical 0 when the majority of inputs are logical 1. A three-input complementary majority function can be expressed in terms of fundamental boolean operators as Eq. 2:

$$\overline{M(a,b,c)} = \overline{ab + ac + bc} \quad (2)$$

The gate symbol of complementary majority gate is illustrated in Fig.3. A majority gate based on SEB is shown in Fig.4 (a). In this structure, two majority gates are serially connected. The first complementary majority gate accepts three inputs and the second one accepts the output of the first complementary majority gate as one of its inputs and the two other inputs of the second majority gate are logic 1 and logic 0, therefore, it plays a role as a NOT gate. Fig. 4(b) shows the simulation results for the proposed three-input majority gate. We divide the gate circuits (as shown in Fig. 4(a)) into two parts, and excite each part in turn by one phase of the two clock signals, θ_1 and θ_2, as shown in Fig. 5.

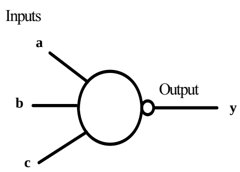
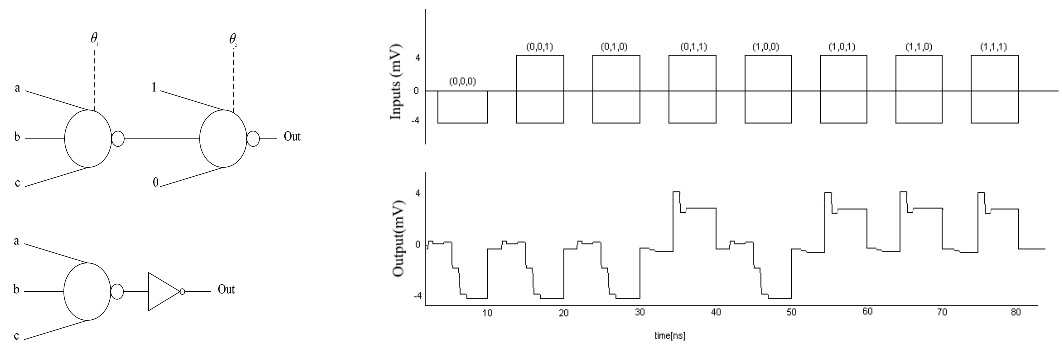


Fig.3. Complementary majority gate symbol.



(a) (b)

Fig. 4. (a) three-input majority gate with two complementary majority gates in series that the second majority acts as NOT gate. Two-step clock pulses controls signal flow (b). Simulation results for three-input majority gate.

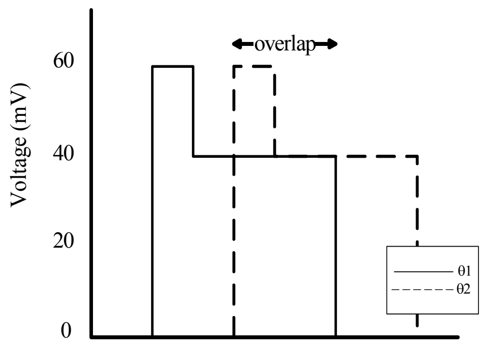
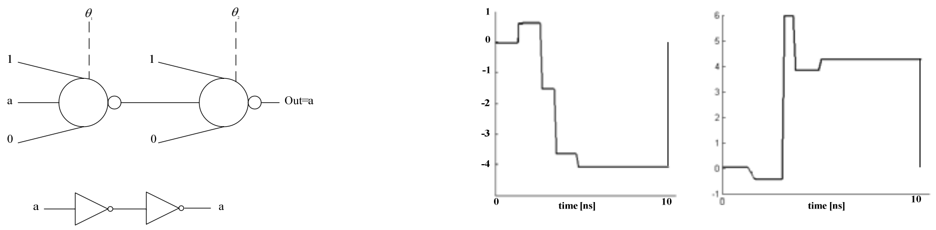


Fig. 5. the two-phase two-step clock pulses used to excite majorities.

3-2 Buffer Gate

Fig.6 (a) shows two majority gates which are connected in series and by applying 4 mV and -4mV which are logic 1 and 0, to the both of them as control inputs, a buffer gate is obtained. In a majority gate, if two of inputs connected to logic 1 and 0 respectively, the output of the gate will be the complement of the third input logic, hence, this gate acts as a NOT gate. If the input is logic 1 the output will be logic 0 and vice versa. Using two NOT gates in series, make buffer gate. The second majority accepts the first majority output as its input. Our proposed buffer accepts an input and then produces an output with the same logic as the input. The simulation results for input logic 0 and 1 are shown in Fig.6.(b).



(a) (b)

Fig. 6. (a) Buffer based on two majority gates in series, and the gate schematic.(b) the simulation results for proposed buffer.

3-3 AND and OR Gates

The proposed three-input cell can configured by applying appropriate logic to the control input in order to acts as an AND gate (Fig. 7(a)) or an OR gate (Fig. 8.(a)). If one of the inputs of the complementary majority function set to 0 ($C=0$), the result function will be a NAND function (Eq. 3):

$$\overline{M(a,b,0)} = \overline{ab} \quad (3)$$

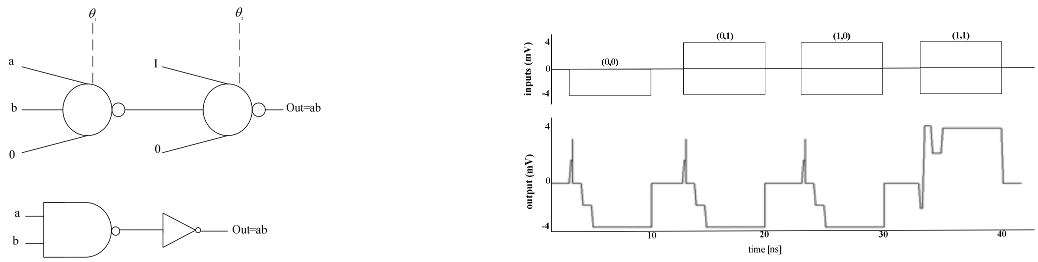
The second majority gate which has two control inputs and accepts logic 1 and logic 0 acts as a NOT gate. In other words, it accepts $\overline{ab}$ and produces ab as its result. Similar to previous sub section, θ_1 and θ_2 are used in order to control the signal flow on the circuit. In order to simulate the AND gate, four sets of inputs (a,b) = (0,0), (0,1), (1,0) and (1,1) were sequentially entered, and the correct outputs (out) = (0), (0), (0) and (1) were produced respectively (Fig.7.(b)). Also, if one of the inputs of the complementary majority function set to 1 ($C=1$), the result function will be a NOR function (Eq. 4):

$$\overline{M(a,b,1)} = \overline{a+b} \quad (4)$$

Similar to the AND gate structure, the second majority gate acts as a NOT gate. In order to simulate the OR gate, the same as the AND gate, four sets of inputs (a,b) = (0,0), (0,1), (1,0) and (1,1) were sequentially entered, and the correct outputs (out) = (0), (1), (1) and (1) were produced respectively (Fig.8.(b)).

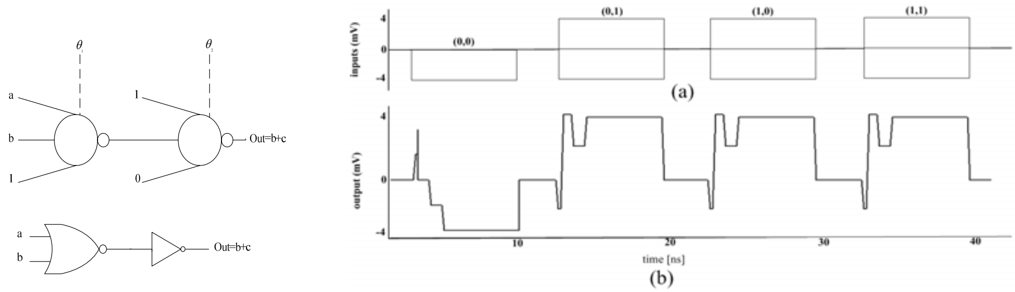
4 A Novel Five-Input Configurable Cell Based on SEB

In this section, a novel five-input cell based on SEB is presented. In comparison with three-input majority gates, implementing a five-input majority gate with conventional digital technologies need more transistors and cause complex design. Fig. 9(a) depicts a five-input majority gate based on irreversible single electron box.



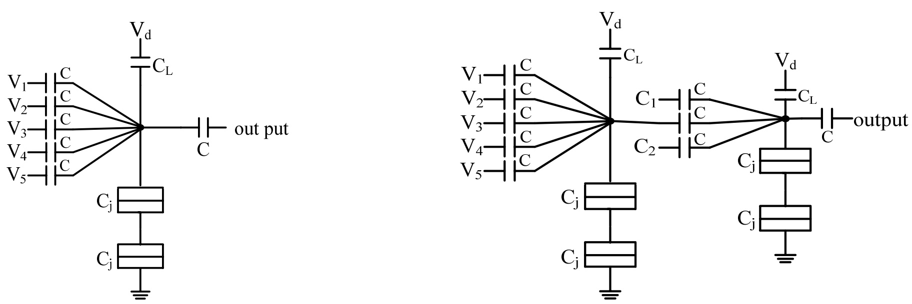
(a) (b)

Fig. 7. (a) The AND gate and the gate schematic. (b) The simulation result for four sets of inputs.



(a) (b)

Fig. 8. (a) The OR gate and the gate schematic. (b) The simulation result for four sets of inputs.



(a)

(b)

Fig.9.(a). A five- input complementary majority gate based on irreversible single electron box. (b) A new five-input configurable cell.

Input voltages V_1, V_2, V_3, V_4 and V_5 in five-input majority should be 4mV or -4mV for representing logic 1 or 0. The bias voltage V_d in complementary majority logic is also a two-step clock pulse which is 60 mV (excitation voltage) and then is set to 40 mV (holding voltage). By exploiting a five-input majority which serially connected to a three-input majority a new cell is presented (Fig. 9(b)).

5 Logic Gate Design Using Five-Input Configurable Cell

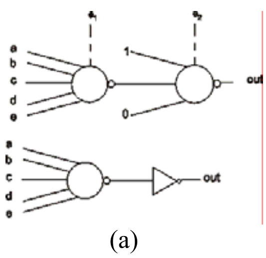
In Section 3, we introduced a three-input majority gate. By connecting two of those majority gates in series, a configurable cell is designed. In this section, another cell based on SEB is introduced. The main difference between this majority and the majority being introduced in Section 3 is the number of inputs as this majority is a five-input one and the previous was a three-input one. This cell is used for design of buffer, five-input majority gate, two-input and three-input AND gates and two-inputs and three-inputs OR gates.

5-1 A Five-Input Majority Gate

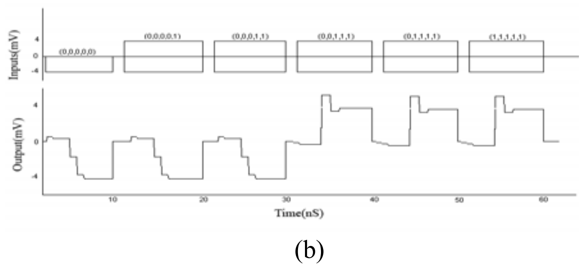
As mentioned in section 3-1, the majority gate can have 3 or more than three-inputs. In this section, a five-input majority gate is proposed. For five inputs a, b, c, d and e, complement of majority function is shown in Eq. 5.

$$\begin{aligned}&\overline{\bar{a}\bar{b}cde+\bar{a}b\bar{c}de+\bar{a}bc\bar{d}e+\bar{a}bcd\bar{e}+\bar{a}bcde+a\bar{b}\bar{c}de+a\bar{b}c\bar{d}e+a\bar{b}cd\bar{e}+a\bar{b}cde+}\\&\overline{ab\bar{c}\bar{d}e+ab\bar{c}d\bar{e}+ab\bar{c}de+abc\bar{d}\bar{e}+abc\bar{d}e+abcd\bar{e}+abcde}\end{aligned} \quad (5)$$

The output of this gate is connected to one of the inputs of a three-input majority gate which the other inputs of the three-input majority gate are connected to logic 1 and 0. The second majority gate, acts as a NOT gate (Fig. 10(a)). We divide the gate circuits into two parts, and excite each part in turn by one phase of the two clock signals, θ_1 and θ_2 .The simulation results for six different sets of input are shown in Fig. 10(b).



(a)

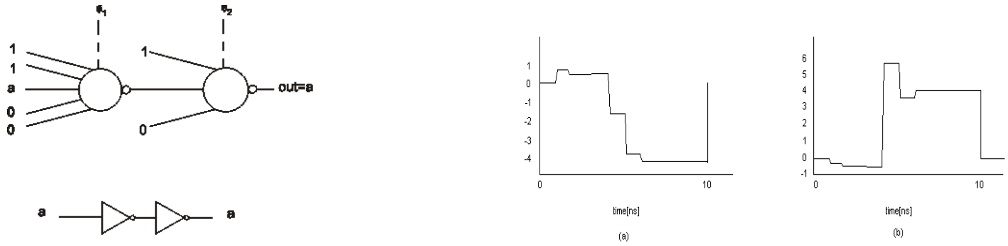


(b)

Fig. 10. (a) A five-input majority gate and the gate schematic. (b) The simulation result for proposed majority gate with five different inputs.

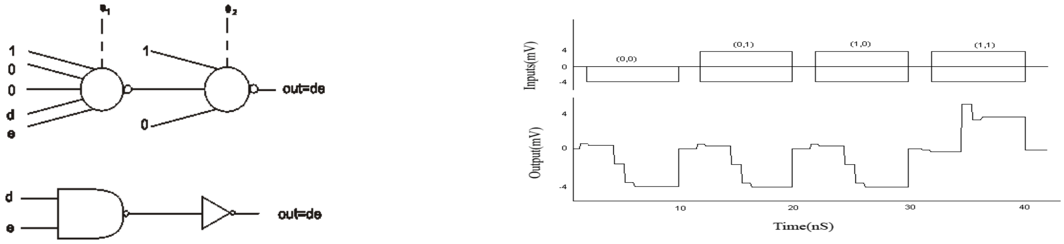
5-2 Buffer Gate

By connecting two complementary majority gates in series a buffer can be designed. In this structure, the first gate is a five-input majority gate which two of its inputs are logic 0 and two of its other inputs are logic 1 and the last input is considered as buffer input. In other words, it acts as a NOT gate. The second majority gate accepts logic 1 and logic 0 for two of its inputs and the third input receives the output of the first gate, therefore, this gate also plays a role as a NOT gate (Fig. 11(a)). The proposed buffer accepts an input and then produces an output with the same logic as the input. The simulation results for input logic 0 and 1 are shown in Fig. 11(b).

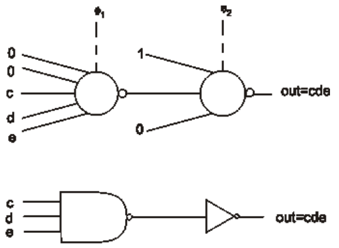


(a) (b)

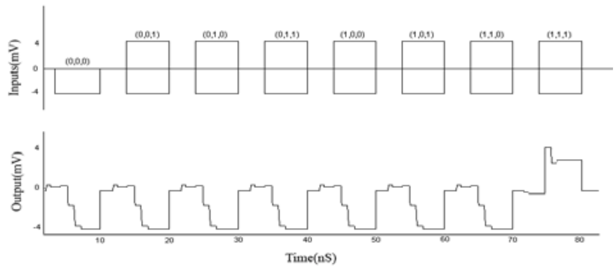
Fig.11. (a) a buffer based on two majority gates in series. (b) The simulation results for the proposed buffer.



(a) (b)



(c)

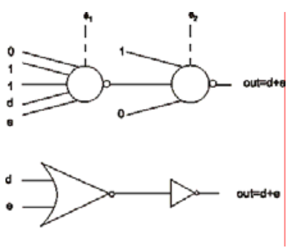


(d)

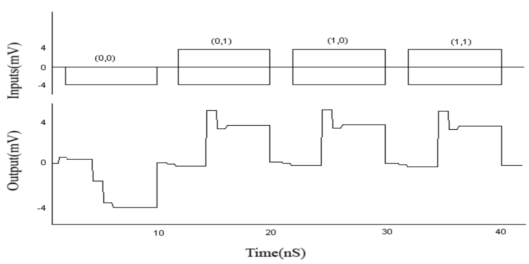
Fig.12.(a) The two-input AND gate and the gate schematic. (b) two-input AND gate simulation for four different sets of inputs. (c) The three-input AND gate and the gate schematic. (d). AND gate simulation for eight sets of inputs.

5-3 AND and OR Gates

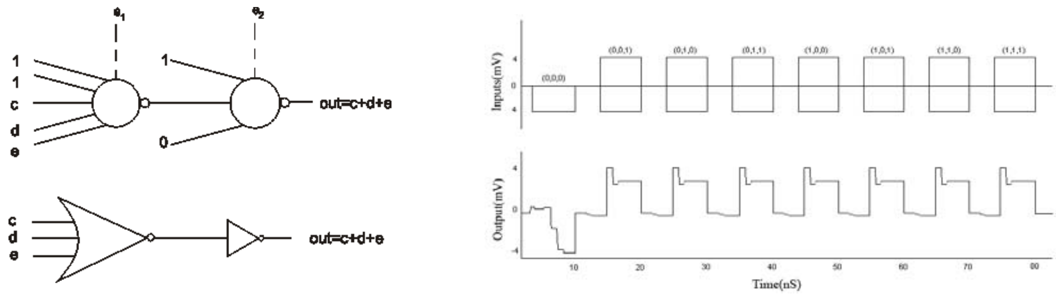
In this section two and three-input AND and OR gates are presented. In order to design the two-input AND gate, one of its inputs is set to logic 1 ($a = 1$) and two remained inputs are set to logic 0 ($b = c = 0$). If $a = 1$ and $b = c = 0$, the boolean function in Eq. 5 will be equal to $\overline{de}$. Fig.12. (a) shows the two-input AND gate and Fig.12.(b) depicts the simulation result for the two-input AND gate. For designing a three-input AND gate, two inputs are set to 0 ($a = b = 0$). Then Eq. 5 will be equal to $\overline{cde}$. Fig. 12(c) shows the three-input AND gate and Fig. 12(d) illustrates the simulation result for the three-input AND gate.
For presenting the two-input OR gate structure, one of its inputs is set to logic 0 ($a = 0$) and the other inputs are set to logic 1 ($b = c = 1$). If $a = 0$ and $b = c = 1$, the boolean function in equation 5 will be equal to $\overline{d + e}$. Fig. 13(a) shows the two-input OR gate and Fig. 13(b) depicts the simulation result for the two-input OR gate. In order to design a three-input OR gate, two inputs are set to 1 ($a = b = 1$). Then Eq. 5 will be equal to $\overline{c + d + e}$. Fig. 13(c) shows the three-input OR gate and Fig. 13(d) illustrates the simulation result for the three-input OR gate.



(a)



(b)



(c) (d)

Fig.13.(a) The two-input OR gate and the gate schematic.(b) two-input OR gate simulation for four sets of inputs. (c). The three-input OR gate and the gate schematic.(d) three-input OR gate simulation for eight sets of inputs.

6 Full Adder

Full adder is a basic arithmetic component which has three inputs and two outputs (typically named sum and carry). If a,b and c are considered as inputs, sum and carry functions in terms of inputs are shown in Eq. 6 and Eq. 7, respectively.

$$sum = (a \oplus b \oplus c) = abc + \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} \quad (6)$$

$$carry = ab + ac + bc \quad (7)$$

Full adders are one the most important parts of each ALU. Any kind of improvements in full adder design result in significant improvement in ALU functionality. Hence different devices are used in order to implement full adders [10-11]. Many different structures for full adder based on single electron devices are proposed in literatures [12-14].

Almost all of the full adders uses majority gates as their main component [4], but differ in the way the majority gates implemented. Pass transistor logic (PTL) [9] and threshold logic gate (TLG) [5] are the other kinds of proposed structures for full adders. Combination of TLG and SET present a new design for full adder called TLG-SET based full adder [3]. In Sections 6-1 two full adders based on previously introduced configurable cells are introduced. The first one is based on five-input configurable cell and the second one is based on three-input configurable cell. In Section 6-2, two full adders are compared.

6-1 Designing Full Adders Using Five-Input and Three-Input Configurable Cells

The block diagram and simulation of a full adder using five-input configurable cells is depicted in Fig. 14. This figure shows the carry (Fig. 14(a)) and the sum (Fig.

14(c)) functions by the use of block diagram in order to illustrate these functions simply. However, the simulation results are shown in Fig. 14(b) and Fig. 14(d) for carry and sum functions respectively. The simulations show that for each set of inputs for carry and sum function, correct output is generated. Also, the block diagram of a full adder using three-input configurable cells are depicted in Fig 15.

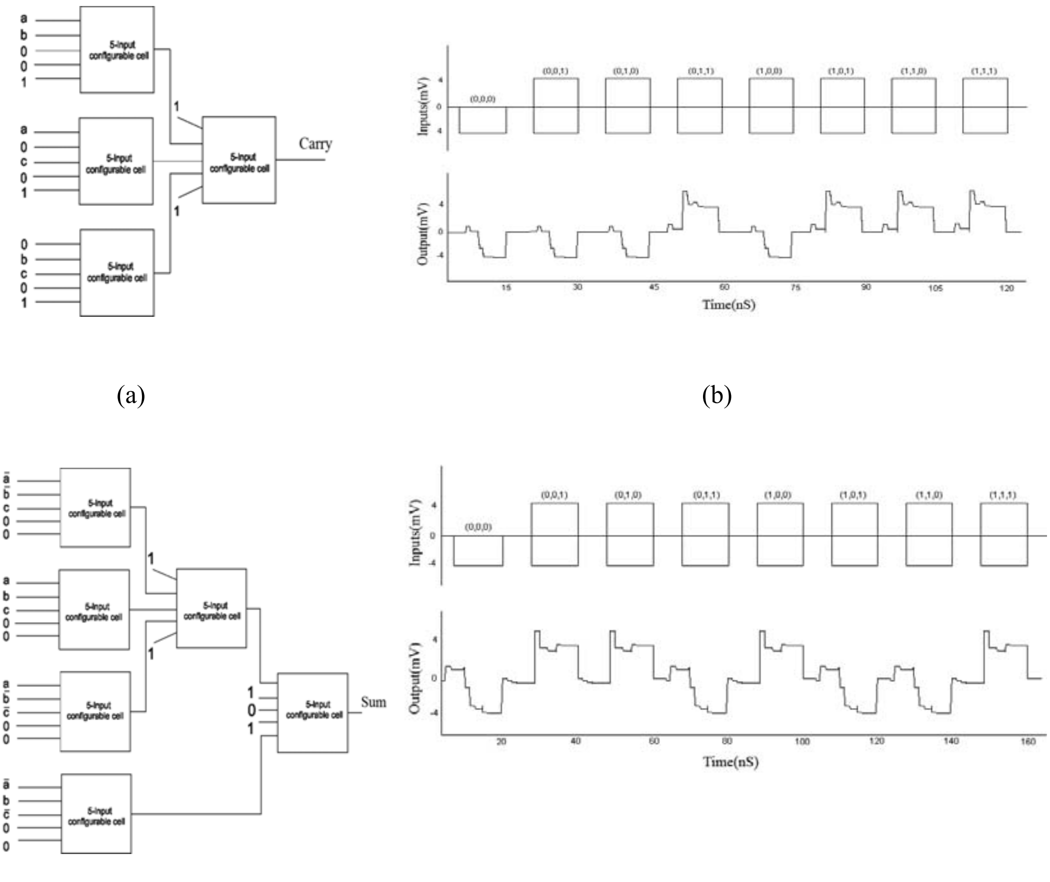
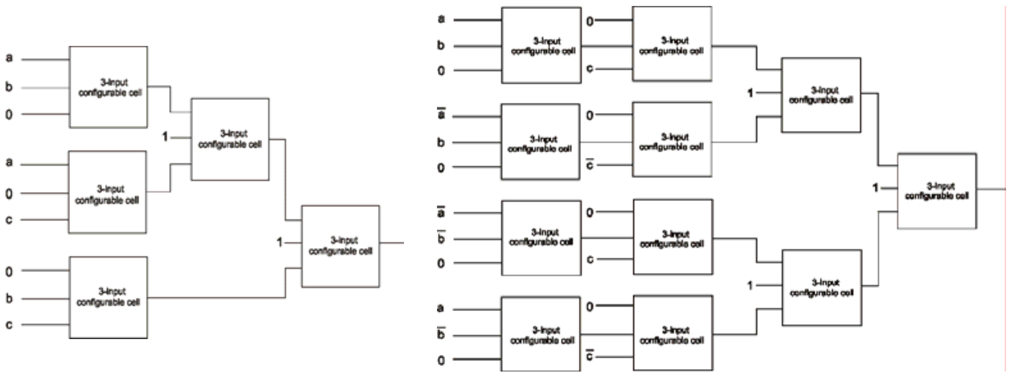


Fig. 14. A full adder block diagram based on five-input configurable cell. (a) Carry function diagram (b) Carry function simulation results (c)Sum function diagram (d)Sum function simulation results.

6-2 Comparing Two Full Adders

A Quantitative comparison of two designed full adders (FA) that depicted in Fig. 14 and Fig. 15, are provided in Table I. Table I shows that full adder made up of five-input configurable cells contains less elements in terms of capacitors and tunnel junctions than the full adder made up of three-input configurable cells. The stages (the cells between the applied inputs and output result) for producing sum and carry function for proposed full adder made up of five-input configurable cells is 2 and 3 stages respectively (Table I). Hence, in comparison with full adder made up of three-input configurable cells, it shows one stage reduction in both sum and carry function that result in less delay.



(a) (b)

Fig. 15. A full adder block diagram based on three-input configurable cell. (a)Carry function diagram (b)sum function diagram.

Table 1. A Quantitative comparison of two designed full adders (FA)

		# of bias capacitors	# of tunnel junctions	# of 5-input complementary majority gates	# of 3-input complementary majority gates	# of stages between inputs and output
3-input configurable based FA	Sum	22	44	-	22	4
	Carry	10	20	-	10	3
5-input configurable based FA	Sum	12	24	6	6	3
	Carry	8	16	4	4	2

7 Conclusions

In this paper we introduce two novel configurable cells based on irreversible single electron box which are suitable for implementing majority, buffer, AND and OR logic gates. These cells are three-input and five-input. By the use of three-input cell we are able to have two input AND and OR gate and also a three-input majority gate. Five-input cell is suitable for two and three-input AND and OR gates besides three and five-input majority gates. As an application, a full adder based on five-input cell is presented and compared with full adder based on three-input cell. The proposed full adders based on five-input cell has a simple structure and consists of a fewer stages between inputs and output in comparison with the three-input one. All the simulations have been performed with SIMON simulator.

References

[1] S. J. Ahn and D. M. Kim, "Asynchronous analogue-todigital converter for single-electron circuits", Electron Lett., vol. 34, no. 2, pp. 172-173, 1998

[2] D. Bahrepour, Naeimeh Soheili, Keivan Navi, Peyman Loloeyan, 'A Configurable Cell Based on Irreversible Single Electron Box,' Proceedings of 13th National CSI Computer Conference, Sharif University of Technology, March, 2008.(in Persian)

[3] M. Haghparast and K. Navi, "Design of a Novel Fault Tolerant Reversible Full Adder for Nanotechnology Based Systems," World Applied Sciences Journal, In Press, 2007

[4] H. Iwamura, M. Akazawa and Y. Amemiya, "Single-electron majority logic circuits, " IEICE Trans. Electron., Vol. E81-C, pp. 42–48, 1998.

[5] C. Lageweg, S. D. Coțofană and S. Vassiliadis, "A full adder implementation using SET based linear threshold gates," Proc. Intl. Conf. Electronics, Circ. and Sys., ICECS'02, pp. 665–668, 2002.

[6] B. H. Lee and Y. H. Jeong, "A Novel SET/MOSFET Hybrid Static Memory Cell Design, IEEE Trans. On Nanotechnol., vol. 3, no. 3, pp. 377-382, 2004.

[7] K. K. Likharev, "Single-elecron Devices and their applications", Proc. IEEE, 87, 606-632 (1999).

[8] K. Navi, M. J. Sharifi, D. Bahrepour and M. Yaghoubi, "High Speed Saturating Counter based on Single Electron Device," 12th Computer Society of Iran (CSI) Computer Conference, March, 2007 (in Persian).

[9] Y. Ono, H. Inokawa and Y. Takahashi, "Binary adders of multi-gate single-electron transistor: Specific design using pass-transistor logic," IEEE Trans. Nanotech., Vol. 1, pp. 93–99, 2002.

[10] M. Rahimi Azghadi, O. Kavehei and K. Navi, "A Novel Design for Quantum-dot Cellular Automat Cells and Full Adders, " Journal of Applied Sciences, Vol. 7, No. 22, pp. 3460-3468, 2007.

[11] M. Sulieman, "Design and analysis of single-electron technology neuralinspired gates and arithmetic circuits," Ph.D. dissertation, School Elect. Eng. Comput. Sci., Washington State Univ., Pullman, 2004.

[12] Y. Takahashi, Y. Ono, A. Fujiwara and H. Inokawa, “Silicon Single-Electron Devices for Logic Applications,” Multiple-Valued Logic (ISMVL 2000), 30th IEEE International Symposium. pp. 411–420. 2000.
[13] C. Wasshuber, H. Kosina and S. Selberherr, “SIMON-A Simulator for Single-Electron Tunneling Devices and Circuits, ” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 9, pp. 937-944, 1997.
[14] “Special issue on limits of semiconductor technology,” Proc. IEEE, vol. 89, Mar. 2001.

Received: October, 2008