Contemporary Engineering Sciences, Vol. 1, 2008, no. 1, 1 - 13

Comparator-Based Switched-Capacitor Delta-Sigma Modulation

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Abstract

In order to eliminate the use of operational amplifiers (opamps) in sampled-data systems and thus avoid several delicate tradeoffs involved with their design, a new class of switched-capacitor circuits based on comparators was reported. The novelty of this comparator-based switched-capacitor (CBSC) design method is the detection of a virtual ground condition rather than forcing it through feedback as in the case of opamp-based systems. In this paper, the previously reported CBSC circuit was extended to a differential configuration. As an application, first- and second-order low-power lowpass discrete-time $\Delta\Sigma$ modulators with CBSC gain stages were designed and their performance evaluated.

Keywords: Comparator-based switched-capacitor circuitry, analog-to-digital conversion, delta-sigma modulation, low voltage, low power

1 Introduction

One of the principal reasons for the dominance of CMOS technology in today's semiconductor market is the scalability of MOSFET devices. As mixed analog-digital circuit designs advance into ever more deeply scaled technology, both the maximum allowable signal swing of the circuit and the intrinsic device gain have been reduced. High gain, however, is important in feedback systems because it determines the accuracy of the output. An essential building block in

CMOS circuit design, particularly affected by these issues, is the operational amplifier (opamp). Various circuit topologies and techniques, with several delicate tradeoffs involved, have been developed to achieve high opamp gain while providing sufficient voltage swing and maintaining the same dynamic range.

A recently reported methodology [6] describes the utilization of comparator-based switched-capacitor (CBSC) circuits in order to eliminate the use of opamps in sampled-data systems. The paper describes a single-ended switched-capacitor gain stage using a comparator and a current source to replace the opamp. The basic principle of CBSC operation is based on the detection of a virtual ground condition in the CBSC case rather than forcing it via feedback in the opamp case. The advantages to this approach are an inherently higher power efficiency, a removal of feedback and stability concerns, and its compatibility to most known opamp-based architectures.

Our work extends the reported topology to a differential CBSC configuration which is used in discrete-time (DT) integrators to design and implement first- and second-order low-power lowpass (LP) DT $\Delta\Sigma$ modulators on the transistor-level in 0.13 µm UMC CMOS technology to show its applicability. The same modulator topologies were also realized with macromodel-based opamps and were additionally modeled in MATLAB. In the end, the simulation results from these three simulation approaches were compared against one another in terms of modulator performance and computational efficiency.

In the remainder of the paper, section 2 introduces the theory of CBSC operation and discusses both the single-ended and differential CBSC circuits. Section 3 presents the used modulator topologies and describes their implementation in CMOS circuitry. Finally, simulation results obtained are shown and discussed in section 4, and the paper concludes with some final remarks in section 5.

2 Comparator-Based Switched-Capacitor Circuits

2.1 Single-Ended CBSC Configuration

Fig. 1 shows a simplified schematic of a practical single-ended CBSC gain stage along with its timing diagram [6]. Continuous-time comparator K1 and current sources I_1 and I_2 have replaced the opamp, which is typically used in a conventional switched-capacitor (SC) gain stage and which forces its input into a virtual ground condition due to its high gain.

The timing diagram in Fig. 1 shows the charge transfer phase indicated by ϕ_2 and is divided into two phases denoted by E_1 and E_2, the *coarse* and *fine*

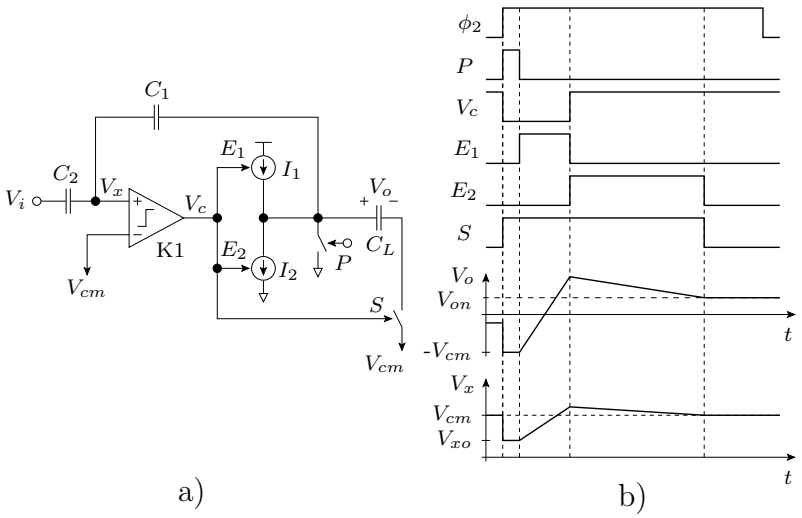


Figure 1: Single CBSC gain stage. a) Charge transfer circuit and b) timing diagram.

charge-transfer phases, respectively. During the sampling phase indicated by ϕ_1, the input voltage, V_i, is sampled onto capacitor C_2, while control signals E_1 and E_2 as well preset P and sampling signal S are low. At the beginning of the charge-transfer phase, a brief preset is performed to clear load capacitance C_L and ensure voltage V_x at the input of the comparator starts below the common-mode voltage, V_{cm}, at a voltage V_{xo}. Further, the voltage across the load capacitance, V_o, drops to $-V_{cm}$. The preset is accomplished by pulling the output node of the circuit to the lowest potential (GND) available. After the preset, the coarse charge-transfer phase starts with the rising edge of control signal E_1. While E_1 is high, the output current source, I_1, charges the load capacitance and leads to a relatively fast voltage ramp on V_x from V_{xo} toward V_{cm}. V_o on the other hand ramps from $-V_{cm}$ toward V_{on} due to the increase of charge on C_L. V_{on} is the same voltage one would obtain when using a conventional SC gain stage with a high-gain opamp and identical capacitance values and is therefore the desired voltage on C_L. Once V_x crosses V_{cm}, the comparator makes its first decision by turning off current source I_1. Because of the finite delay of the comparator, I_1 is turned off after V_x has already crossed V_{cm} and thus leads to an overshoot of V_x by a certain voltage as shown in Fig. 1 b). To compensate for this overshoot effect, current source I_2 is now turned on. The current provided by I_2 is less than that of I_1 and therefore results in a slower voltage ramp of V_x toward V_{cm}. Likewise, output voltage V_o ramps down to V_{on} due to the decrease of charge on C_L. Once V_x crosses V_{cm} again, now in the opposite direction, the comparator turns off I_2 and opens the sampling switch as indicated by the falling edge of signal S. The desired charge is sampled on C_L at that point and signal S therefore defines

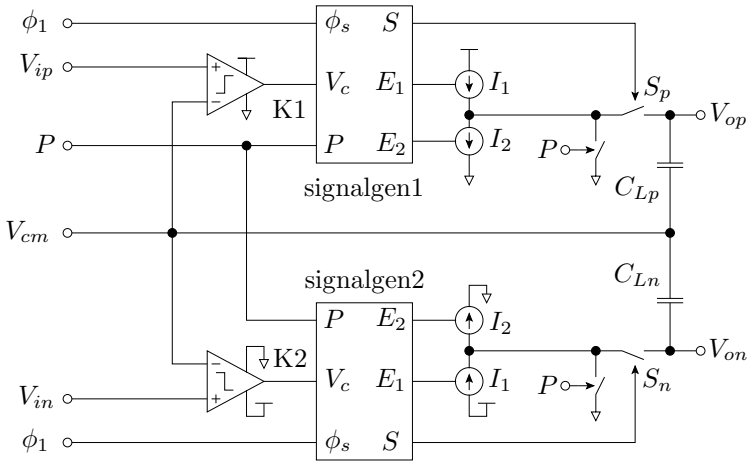


Figure 2: Differential CBSC gain stage.

the sampling instant. The final overshoot caused by the comparator delay in turning off I_2 is smaller than the previous overshoot due to the much slower voltage ramp and, additionally, is a constant offset if the ramp rate and the comparator delay are constant. Apart from comparator delay, offset and clock jitter also affect the voltage overshoot. Both offset due to device mismatch and comparator delay result in signal-independent errors that can be corrected, while clock jitter is a statistical source of error that can be modeled as an additional noise source.

From this description of the CBSC gain stage in Fig. 1, one can clearly differentiate the two different principles of operation: While an opamp-based design *enforces* a situation in which V_x is equal to V_{cm}, the comparator-based design *detects* such a virtual ground condition whenever V_x crosses V_{cm}. Because of this way of operation, it is expected that CBSC circuits are more power efficient than conventional opamp-based circuits. Furthermore, the output settles to the same voltage in the sampling instant in both cases. This indicates that CBSC circuits are potentially compatible to most opamp-based topologies, which is later shown for the case of a $\Delta\Sigma$ modulator.

2.2 Differential CBSC Configuration

Differential circuitry has several important advantages over single-ended circuitry, such as higher immunity to noise sources, an increase in maximum achievable signal swings, higher linearity, and lower distortion. For these reasons, we have developed a differential version of the single-ended CBSC gain stage in Fig. 1, which is shown in Fig. 2. The symbol which is used for this circuit in later schematics is shown in Fig. 3. Note that V_{SS} is held at ground potential throughout all simulations while V_{DD} is held at 1.2 V.

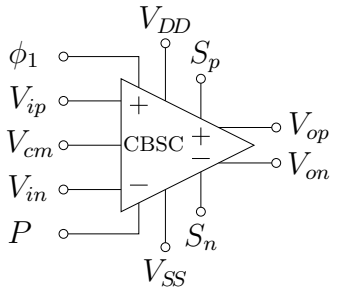


Figure 3: Symbol of the differential comparator-based switched-capacitor circuit. Note that since V_{DD} and V_{SS} are held at constant values of 1.2 V and 0 V, respectively, they are omitted in subsequent schematics.

The signal generators, signalgen1 and signalgen2, are explicitly shown in Fig. 2 to indicate that signals E_1, E_2, and S are digitally generated to control current sources I_1 and I_2 as well the sampling instant. The signal generators are asynchronous logic circuits designed to perform these tasks based on the sampling phase, ϕ_1, the comparator output, V_c, and the preset, P. Two symmetrically arranged single-ended CBSC gain stages constitute the differential CBSC gain stage with a differential voltage, $V_{ip} - V_{in}$, at its input.

The operation of this circuit is similar to the operation of its single-ended counterpart. While voltage V_{ip} is compared to the common-mode voltage at the input of comparator K1 of the upper CBSC gain stage, voltage V_{in} is used in the lower gain stage. Load capacitors C_{Lp} and C_{Ln}, connected back to back with V_{cm} as the common node, are then charged or discharged separately by the two sets of current sources. The differential output, $V_{op} - V_{on}$, is then taken across these capacitors.

In the following, the differential comparator-based switched-capacitor gain stage in Fig. 2 is used in a first- and second-order $\Delta\Sigma$ modulator.

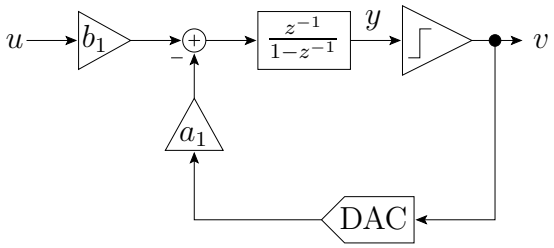
3 Modulator Topology and Circuit Implementation

3.1 Modulator Topology

The topologies for the first- and second-order $\Delta\Sigma$ modulators are shown in Figs. 4 and 5, respectively. Coefficients are determined using the MATLAB $\Delta\Sigma$ Toolbox [4].

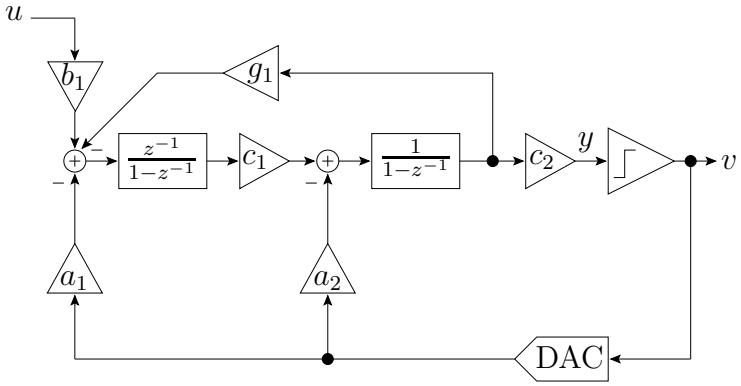
Note that coefficient c_2 is unimportant since the quantizer is single-bit. All coefficients that are not represented in these figures are equal to zero.

In the following subsection, the implementation of the modulator block diagrams in CMOS circuitry is described.



$a_1 = 0.275$
$b_1 = 0.275$

Figure 4: Ideal first-order $\Delta\Sigma$ modulator.



$a_1 = 0.176$
$a_2 = 0.137$
$b_1 = 0.176$
$c_1 = 0.181$
$c_2 = 3.927$
$g_1 = 0.003$

Figure 5: Ideal second-order $\Delta\Sigma$ modulator.

3.2 Circuit Implementation

As can be seen in Figs. 2, 4, and 5, two of the required circuit blocks are a comparator to be used in the CBSC gain stage and a clocked comparator with a latch to be used as the single-bit quantizer in the modulator [1]. A single-bit quantizer is employed because of its inherent linearity, ease of implementation, and to avoid harmonic distortion due to a mismatch in the step size of multibit quantizers. As already indicated, the use of differential configurations comes with several important advantages, such as cancellation of all even-order distortion terms (harmonic and intermodulation), regardless of the cause of the distortion, reduced clock feedthrough and charge injection due to switching, higher linearity and increased dynamic range.

The voltage comparator is shown in Fig. 6. It consists of a preamplification stage, a decision circuit, and an output buffer. The preamplification stage (M_1–M_7) is a differential amplifier (diff-amp) with active loads suitable for high speed since there aren't any high-impedance nodes other than the input and output nodes. The decision circuit (M_8–M_{12}) uses positive feedback from the cross-gate connection between M_9 and M_{10} to increase the gain of the decision element and includes a transistor, M_{12}, which acts to shift the output level of the decision circuit upward and thereby moves it into the common-mode range of the output buffer. Finally, the output buffer or postamplification stage

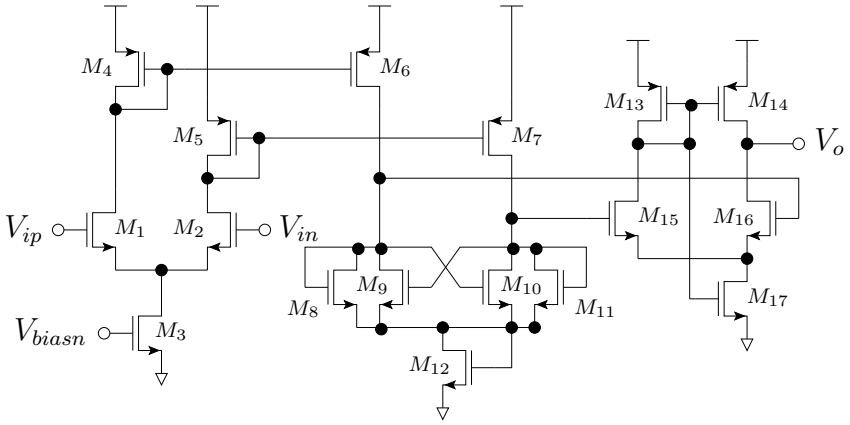


Figure 6: Comparator (bias circuit not shown). Aspect ratios are: M_1–M_2 = 2.4 µm/120 nm; M_3, M_{17} = 2.4 µm/240 nm; M_4–M_5, M_{15}–M_{16} = 600 nm/240 nm; M_6–M_7 = 600 nm/480 nm; M_8–M_{11} = 240 nm/240 nm; M_{12} = 240 nm/120 nm; M_{13}–M_{14} = 1.2 µm/240 nm.

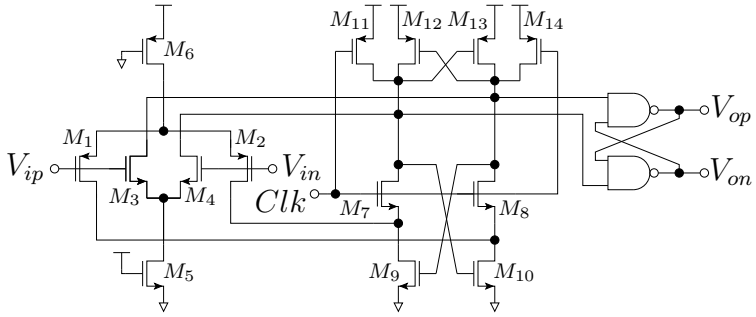


Figure 7: Wide-swing clocked comparator with NAND SR latch. All NMOS are W/L = 1.2 µm/120 nm, all PMOS are W/L = 2.4 µm/120 nm, except M_5 = 1.2 µm/1.2 µm and M_6 = 2.4 µm/1.2 µm.

(M_{13}–M_{17}) is used to convert the output of the decision circuit into a logic signal and consists of a simple self-biased diff-amp that is used to regenerate the signal.

The clocked comparator is shown in Fig. 7. It consists of an input stage, the core comparator circuitry and a latch. The input stage (M_1–M_6) consists of two diff-amps, each of which is biased with a current supplied by a long-length transistor, M_5 and M_6, respectively. In the core circuit of the clocked comparator (M_7–M_{14}), M_9–M_{10} and M_{12}–M_{13} form a cross-coupled latch while M_7, M_8, M_{11} and M_{14} are used to actively drive all nodes of the latch to a known voltage. When Clk goes low, M_{11} and M_{14} turn on, pulling the drains of M_{12} and M_{13} as well as the gates of M_9 and M_{10} to V_{DD}. M_7 and M_8 on the other hand are turned off so that the drains of M_9 and M_{10} are actively driven

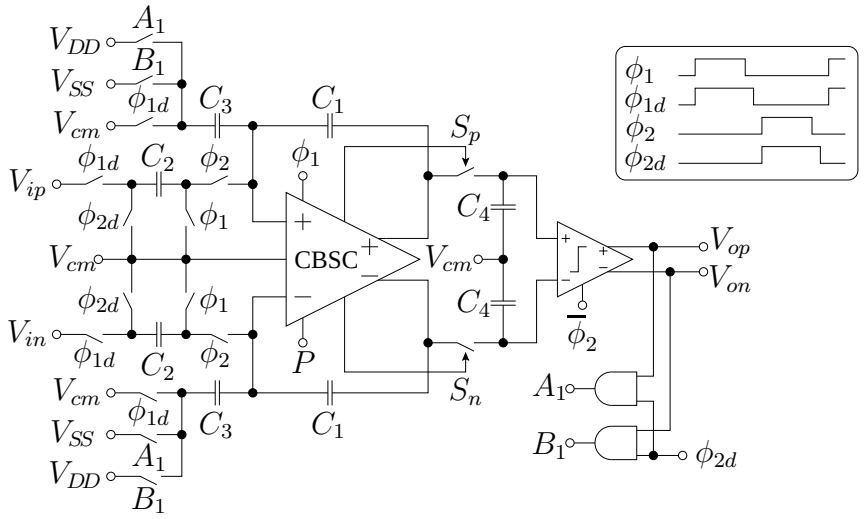


Figure 8: SC implementation of the first-order CBSC $\Delta\Sigma$ modulator and clocking scheme.

to ground. When Clk goes high, the imbalance created by the input diff-amps causes the circuit to latch high or low depending on the state of the inputs. The SR latch is added at the output of the comparator so that the outputs, V_{op} and V_{on}, change state only at the rising edge of the clock signal, Clk.

After proper scaling and denormalization of the signals, the block diagrams of Figs. 4 and 5 were translated into practical circuits for the $\Delta\Sigma$ modulators.

Fig. 8 shows the first-order $\Delta\Sigma$ modulator and the used two-phase non-overlapping clock in detail. Note that, apart from the load capacitors C_4 at the output of the differential CBSC stage, which is used in the parasitic-insensitive integrator, the circuit is identical to an opamp-based topology. Since $a_1 = b_1$, $C_2/C_1 = C_3/C_1$ and the same capacitor may be used to implement the two coefficients. As shown in the schematic, the input is sampled onto capacitors C_2 during ϕ_1, and the difference between the input and the reference is integrated onto capacitors C_1 during ϕ_2. The 1-bit quantizer implemented by the clocked comparator takes the voltage across the two load capacitors C_4 and feeds back its output, V_{op} and V_{on}, through the DAC formed by the ϕ_2 switches and capacitors C_3.

Fig. 9 shows the second-order $\Delta\Sigma$ modulator in detail [3, 2]. As shown in the schematic, a distributed two-level DAC, two comparators, and two parasitic-insensitive switched-capacitor integrators form the second-order modulator. Due to the delaying/non-delaying configuration of the integrators it is possible to use the load capacitors of the first stage as the sampling capacitors of the second stage. During phase 1, the ϕ_1 switches conduct so that the differential input is sampled onto the first integrator's sampling capacitors, C_1. In the second stage, capacitors C_7 are connected to V_{DD} or V_{SS}, depending on

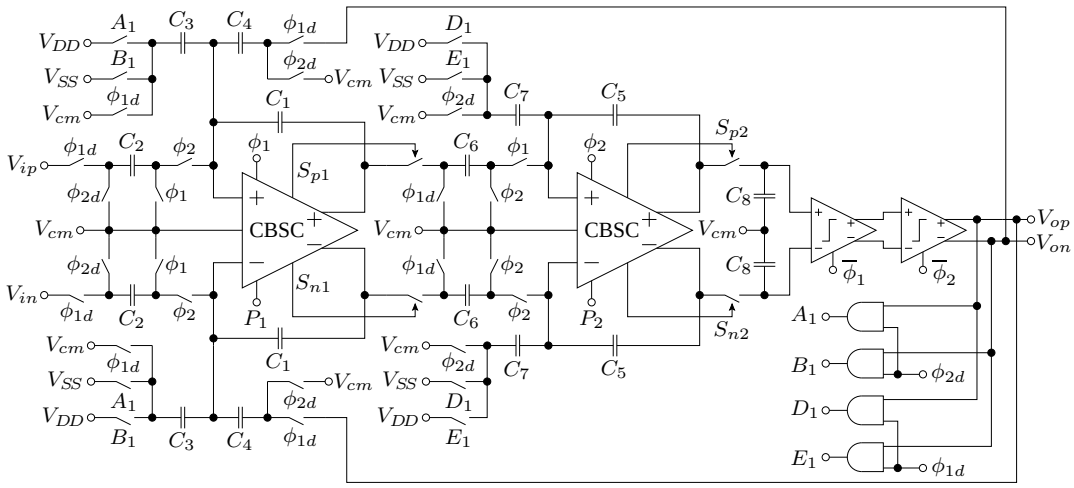


Figure 9: SC implementation of the second-order CBSC $\Delta\Sigma$ modulator.

the result of the comparison from the previous phase. As a result, a packet of charge proportional to the difference of this charge and the charge on sampling capacitors C_6 of the second integrator due to the differential output of the first integrator, is transferred to capacitors C_5. Likewise, during phase 2, the ϕ_2 switches conduct and the D/A conversion and subtraction function now take place in the first stage while the second stage's output voltage does not change so that the comparator at its output is strobed.

Circuit simulations were performed and compared against MATLAB simulations to check the timing, topology, capacitor ratios and impulse response of the circuits and thus verify their proper operation. The following section presents the results obtained with the proposed CBSC $\Delta\Sigma$ modulators.

4 Results and Discussion

The modulators proposed in section 3 have been realized in three different ways: an ideal MATLAB model based on the $\Delta\Sigma$ toolbox, modulators implemented with macromodel-based opamps, and, finally, modulators using CBSC gain stages. This section compares the simulation results obtained with these simulation approaches and evaluates both modulator performance and computational efficiency.

Table 1 summarizes important modulator and performance parameters for the CBSC case while Figs. 10 through 13 plot the output spectra. Both the CBSC and opamp-based modulators are operated at a power supply voltage of 1.2 V and sampled at a frequency, f_s, of 8 MHz. Together with an oversampling ratio, OSR, of 64, this yields a signal bandwidth, f_B, of 62.5 kHz. The

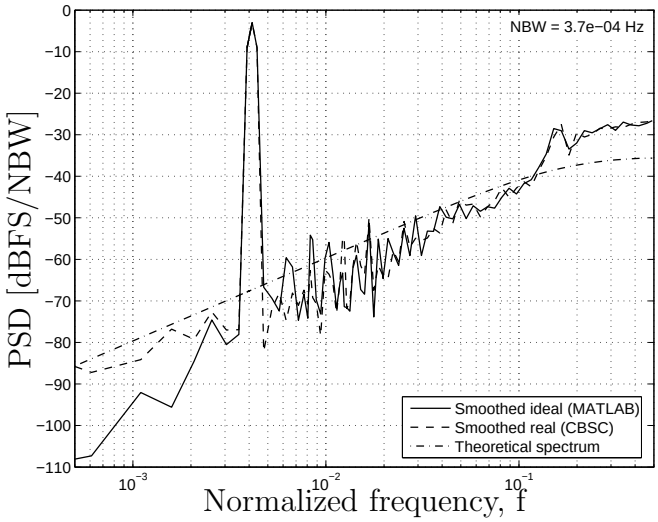


Figure 10: First-order $\Delta\Sigma$ modulator, MATLAB vs. CBSC.

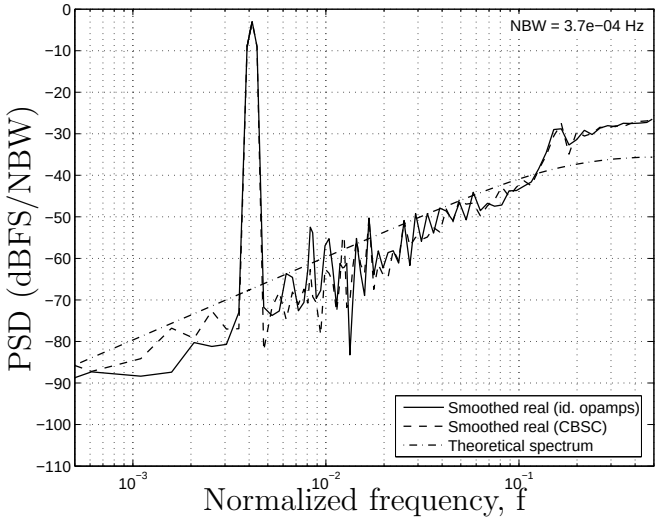


Figure 11: First-order $\Delta\Sigma$ modulator, opamp vs. CBSC.

simulated power dissipation of the first-order CBSC modulator is 121.4 µW while that of the second-order modulator is 253.5 µW. To compute the power spectral density of the modulators, their output was windowed using a Hann window to minimize noise leakage and the number of FFT data points was chosen to be 4096 (64×OSR) based on accuracy and repeatability specifications in estimating the SNR and observing a sufficient spurious-free dynamic range (SFDR) [5]. As confirmed in Figs. 10 through 13, the spectrum of the modulators are in very good agreement to one another and very close to the theoretical spectrum. At an OSR of 64, a noise bandwidth, NBW, of 0.023 Hz, an input

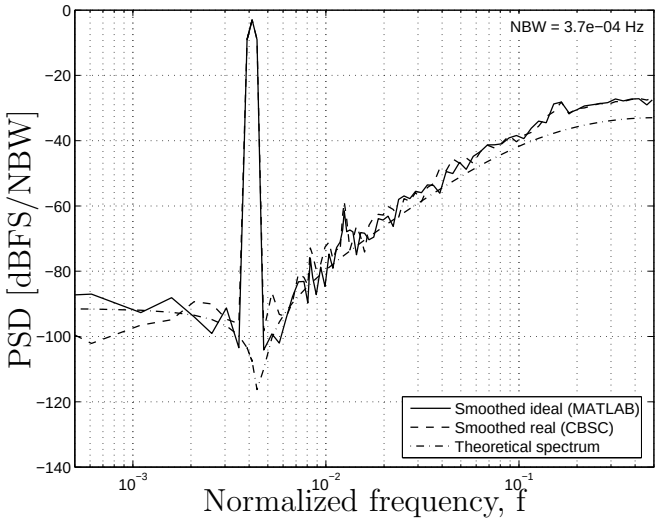


Figure 12: Second-order $\Delta\Sigma$ modulator, MATLAB vs. CBSC.

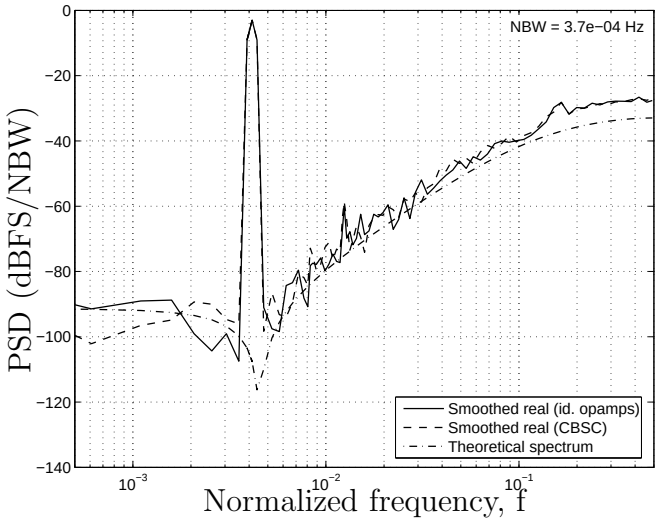


Figure 13: Second-order $\Delta\Sigma$ modulator, opamp vs. CBSC.

signal frequency of approximately 33.20 kHz, and an input signal amplitude of -3 dBFS, the obtained values for the SNDR of the first-order (second-order) modulator are 56.7 dB (71.3 dB) in the CBSC case, 55.4 dB (70.6 dB) in the opamp-based case, and 52.0 dB (73.1 dB) using MATLAB simulations.

5 Conclusion and Future Work

Using CBSC rather than opamp-based modulators comes with several advantages with the most important ones being a significantly smaller area and

Table 1: Performance Summary of CBSC ΔΣ Modulators

ΔΣ *modulator*		DT, LP, 1 bit	
		1st order	2nd order
Sampling frequency		8 MHz	
Signal bandwidth		62.5 kHz	
Oversampling ratio		64	
Power supply		+1.2 V single supply	
Process		UMC 0.13 µm CMOS process	
SNDR[1]	CBSC	56.7 dB	71.3 dB
	Opamp	55.4 dB	70.6 dB
	MATLAB	52.0 dB	73.1 dB
Power consumption[1]		121.4 µW	253.5 µW

[1] For a -3 dBFS input

power consumption up to a factor of 10 while achieving similar dynamic performance, a higher linearity due to the elimination of nonlinearities caused by opamp settling time, and the utilization of similar modulator topologies as in the case of opamp-based implementations.

We have designed and implemented a first- and second-order modulator on the transistor level and shown both proper operation and their agreement to conventional modulators modeled in MATLAB and implemented with macromodel-based opamps.

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Received: January 17, 2008