Impact of FinFET with Plural Number of Channel width Using Novel One Step of Trench Formation Process on Fabrication Cost for System LSI

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Abstract

Impact of FinFET with plural number of channel width using novel one step of trench formation process on fabrication cost for system LSI has been described. Novel one step of trench formation process are realized by using trench etching process for various sizes of trench openings and dummy pattern between adjacent trenches. With these technologies fabrication cost of cell library for system LSI can be reduced to 11-15% compared with that of conventional planar transistor process. Proposed technologies are promising candidate for realizing future high density system LSI design with cell library.

Keywords: 3D NAND flash memory, system LSI, cell library, trench process

1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem FinFET which use the 3 planes as the channel for reducing the short channel effect has been developed [2] [3]. By using FinFET not only reduction of
the short channel effect but also the reduction of the pattern area compared with those of the conventional planar transistor can be realized[4][5].

The structure of FinFET is shown in Fig.1. Not only the planar region but also the sidewalls can be used as the channel. Within the small pattern area large total channel width of WP+2WD can be successfully realized. Because of these features Intel firstly produces FinFET on commercial basis as the high end CPU in 2012[6]-[8]. In these researches only one kind of sidewall channel width is adopted within a LSI to simplify the process technology. One kind of sidewall channel is formed by using one step of trench formation process. In this case large channel width can be realized using plural number of FinFET connected in parallel as shown in Fig.2 (a). This leads to the increase of pattern area. In Fig.2 the cases of Wb=2D+F, 4D+2F, 6D+3F, and 8D+4F are shown.

Fig. 1 Structure of FinFET.

Fig. 2 Cross section of FinFET for large channel width. (a) conventional scheme with one kind of channel width, (b) plural number of trench depth scheme with plural steps of trench formation, (c) proposed scheme.
In order to overcome the inherent increase of pattern area with one step of trench formation process, \( N \geq 2 \) steps trench formation process has been proposed as shown in Fig.2 (b) [9]. For realizing the \( N \) kinds of sidewall channel width \( N \) steps of trench formation process has been adopted. This scheme can reduce the pattern area compared with that of one step of trench formation process. However, this scheme results in the increase of the number of process steps compared with that of one step of trench formation process. If \( N \geq 5 \) is employed, the increase of process cost due to this increase of the number of process steps becomes larger than the reduction of process cost caused by the reduction of pattern area [9]. In the actual system LSI the kinds of channel width of transistor are more than 5 for realizing high speed or low power characteristics [10]-[12]. Therefore, \( N \geq 2 \) steps trench formation process can not be easily introduced to the actual system LSI.

In order to overcome the inherent increase of process steps with \( N \geq 2 \) steps trench formation process, novel process technology which realizes various \( N \geq 2 \) kinds of channel width using only one step trench formation process has been proposed as shown in Fig.2 (C) [9]. Novel process technology can be realized using various small trench opening sizes which is smaller than feature size, \( F \). Various depth of trenches can be successfully realized using only one step trench formation process using various size of trench opening sizes as shown in Fig.3 [13]. However, Ref [9] described

![Image of trench etching process for DRAM capacitor](image_url)

Fig. 3 Trench etching process for DRAM capacitor. Experimental cross sectional view of various trench depth of trenches which are successfully formed with various kinds of trench opening sizes.

Only the simple concept of this novel process technology. The actual process technology featured with novel one step of trench formation technology and the reduction of pattern area, and fabrication cost of the actual system LSI have not been reported.
In this paper the actual process technology for realizing novel one step of trench formation technology and reduction of pattern area, and fabrication cost of the actual system LSI have been newly described. Furthermore, the reduction of pattern design time for system LSI with this scheme has been newly estimated. This paper is organized as follows. Section 2 describes the actual process technology for realizing novel one step of trench formation technology (novel process technology). Section 3 describes the process steps for novel process technology. Next actual pattern area and process cost reduction with novel process technology are shown. Finally, conclusion of this work is provided in Section 5.

2 Actual process technology for novel process technology

As shown in the previous section actual system LSI is composed with various size (channel width) transistors. For example, in the case of System LSI for communication[10], buffer circuit[11] and cell library[12] channel width is distributed from 3F to 43F, which is corresponding to from F where F=(3F-F)/2 to 21F where 21F=(43F-F)/2 for trench depth(Fig.4).

Fig. 4 Distribution of channel width and trench depth for actual system LSI, (a) system LSI for communication, (b) buffer circuit, and (c) cell library.

For the novel process technology by using 1 step process technology trench depth from F to 21F must be successfully fabricated. The corresponding trench size is assumed to be around from 0.3F to F. By using the trench formation technology
for high density capacitor for DRAM, relationship between trench size (trench opening size) and trench depth is shown in Fig.3. Relatively deep trench, from 20F to 28F, has been fabricated. In this case shallow trench from F to 19.9F cannot be fabricated. This is because with decreasing the trench size the aspect ratio increases rapidly from 25 to 52. In order to overcome this problem the polishing of substrate after formation of trench can be introduced. However, with this polishing only shallow trenches, from F to 11F, can be fabricated (Fig.5). Namely, with trench formation technology for high density capacitor for DRAM sufficient wide trench depth range, from F to 21F, can not be fabricated.

This problem can be solved using another kind of trench formation technology, for example, MEMs process (Fig.6) [14]. The value of aspect ratio is large of around 32 and the trench depth dependence on trench size is relatively small as shown in Fig.6. Therefore, relatively wide trench depth range, from 12.5F to 35F can be fabricated. As a result, using the polishing of substrate after formation of trench sufficient wide trench depth range, from F to 21F, can successfully fabricated as shown in Fig.7. Relationship between trench depth vs. trench size with MEMS process + polishing of substrate are shown in Fig.8. For Fig.4 novel process technology can be successfully adopted. In the case that more wider trench depth distribution is required, another trench formation technology which enable to realize higher aspect ratio must be introduced.
Fig. 6 Experimental cross sectional view of various trench depth of trenches width MEMS process.

Fig. 7 MEMS process + polishing of substrate. Dashed line shows polished surface of substrate.
Fig. 8 Relationship between trench depth vs. trench size with MEM Sprocess + polishing of substrate.

3 Process steps for novel process technology

The process steps of novel process technology is shown in Fig.9(a). Two adjacent transistors, channel width of W1 and W2, are shown in simplicity. For realizing channel width of W1, trench depth of (W1-F)/2 is required. The trench size for realizing trench depth of (W1-F)/2 can be easily obtained by using the relationship between the trench size and trench depth. This procedure is written as (trench size)=f(trench depth). The characteristics of Y=f(x) depends on the process technology for trench formation. In the case of Fig.7

Fig. 9 Process step of novel process technology (a) top view, (b) cross sectional view.
Process technology for MEMs has been used. For example, in the case that W1=5F and W2=19F, f((W1-F)/2)=f(2F)=0.33F and f((W2-F)/2)=f(9F)=0.55F are obtained in Fig.8. The depth of trench of adjacent transistor, for W1 and W2, become different value. In order to separate these two trenches dummy pattern of minimum size of F (maximum size of 3F) is newly introduced. After the formation of trench the pattern area of the dummy pattern is oxidized for realizing the isolation area. The cross-section after the trench formation and the oxidation of the dummy pattern are shown in Fig. 9(b). For designing the system LSI used maximum trench size becomes F. Therefore, the maximum distance between active area of adjacent transistor becomes (maximum trench size)*2+(minimum dummy pattern size)=2*F+F=3F. For realizing the flexible pattern design method which is described in the next section this fixed value of 3F is used within the whole system LSI. In the case of conventional system LSI this distance between two adjacent active area is as small as F. Therefore, this large size of 3F results in the larger pattern area compared with that of conventional system LSI. However, as shown in Fig. 10 [15] the distances between two adjacent active area of actual system LSI are larger than 3F in the typical case. This is because for the actual system LSI, well isolation, contact, wiring are located between two adjacent active area as shown in Fig.10. Therefore, for the estimation of pattern area of the next section, it is assumed that the extra pattern area is not required for introducing novel process technology.

4 Actual Pattern area and process cost reduction with novel process technology

In this section reduction of pattern area and fabrication cost of actual system LSI ref[12] by using novel process technology have been described. In this system LSI fabricated with the planar transistor the distance between adjacent transistors is
larger than 3F. Therefore, for the estimation of pattern area only transistor region which corresponds to the active area is taken into account. The pattern area and process cost estimation with conventional FinFET and plural number of FinFET fabricated using plural number of trench process steps have been already described in ref[9]. It is assumed that additional process cost for the formation of one trench process is about 3-5%, the fabrication cost, which is in proportion to the pattern area and the number of process steps, is shown in Fig.11. In the conventional FinFET case the process cost can be reduced to 28-31% compared with that with planar transistor. In the case of plural number of FinFET fabricated using 2 times of trench process steps, the process cost can be reduced to 25-28% compared with that with planar transistor. This value is a little smaller than the conventional FinFET case. If the trench process steps becomes larger than 3, the process cost increases. This is because the increase of cost due to the increase of process steps encounters the reduction of cost due to the reduction of pattern area. On the other hand in the case of novel process technology all kinds of channel width (20, in this case,) can be successfully fabricated using one time of trench formation followed by the oxidization of dummy pattern. Therefore, with novel process technology the pattern area can be reduced to only 11.3-15.5% compared with that with planar transistor. As a results, the process cost with the novel process technology can be reduced to 11-15 % compared with that with planar transistor as shown in Fig.11. This small value is about half compared with that of with 2 times of trench process steps. (the pattern area with the novel process technology is about 43-54% compared with that of with 2 times of trench process steps). These results shows that the novel process technology is promising candidate for reducing the process cost of actual system LSI drastically. The results for that additional process cost for the formation of one trench process is about 3% are summarized in Fig.11.

<table>
<thead>
<tr>
<th></th>
<th>Planar</th>
<th>Conventional FinFET</th>
<th>Planar number of FinFET</th>
<th>Novel process technology</th>
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<tr>
<td>Patten area</td>
<td>1</td>
<td>28.8-31.9%</td>
<td>25.8-28.8%</td>
<td>11.3-15.5%</td>
</tr>
<tr>
<td>number of process steps</td>
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<td>1+2*0.03</td>
<td>1+1*0.03</td>
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<tr>
<td>process cost</td>
<td>100%</td>
<td>28-31%</td>
<td>25-28%</td>
<td>11-15%</td>
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Fig. 11 Pattern area and process cost comparison.

5 Conclusion

Impact of FinFET with plural number of channel width using novel one step of
trench formation process on fabrication cost and pattern design time for system LSI has been described. Novel one step of trench formation process are realized by using trench etching process for various sizes of trench openings and dummy pattern between adjacent trenches. With these technologies fabrication cost of cell library for system LSI can be reduced to 11-15% compared with that of conventional planar transistor process. Proposed technologies are promising candidate for realizing future high density system LSI design by using cell library.

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