Proposal of Stacked Type Fe-FET Reconfigurable Logic Circuit Featured with Parallel Processing Within One Silicon Pillar Using Modified Process Technology of 3D NAND Flash Memory

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Abstract

In order to realize the parallel processing within one silicon pillar, a novel stacked type Fe-FET reconfigurable logic circuit featured with parallel processing within one silicon pillar using modified process technology of 3D NAND flash memory has been newly proposed. For realizing the proposed scheme plural numbers of logics are generated within one silicon pillar. Furthermore, the outputs of these logics are connected to horizontally running wires and these wires are connected to vertically running wires which act as the output signals. For realizing this structure two improvements for fabrication scheme of 3D NAND flash memory should be introduced. First is fabrication process featured by various depth trench formation technology with one fabrication step. Second is connection technology between the output of logic block generated within the silicon pillar to horizontal running wires.

Keywords: NAND type memory, Fe-FET, vertical transistor, parallel processing, logic LSI, reconfigurable architecture, high speed operation
1 Introduction

Recently, the scaling of the conventional planar transistor becomes increasingly difficult because of its large short channel effect [1]. In order to overcome this problem FinFET[2][3] which use the 3 planes and SGT (Surrounding Gate Transistor) [4] which use the 4 planes as the channel for reducing the short channel effect has been developed. By using SGT not only reduction the short channel effect but also the reduction of the pattern area compared with that of the conventional planar transistor can be realized. This is because not only the planar region but also the sidewall can be used as the channel for this newly proposed structure.

The structure of SGT is shown in Fig.1. Four sidewalls can be used as the channel. Assuming that the sidewall channel width is defined as Ws, within the small pattern area large total channel width of 4Ws can be successfully realized. The drain current flows along vertical direction which is perpendicular to the conventional planar transistor case.

![Figure 1: Structure of 1 layered SGT](image)

Firstly, the research of LSI with 1 layered SGT is focused on the device technology of transistor and memory such as DRAM [5]-[9] and system LSI [10]-[11].

Recently, this SGT has been successfully applied to the vertically stacked type system LSI [12]-[13]. The applied vertically stacked type NAND/NAND array is shown in Fig.2. NAND logic is formed within the silicon pillar in which the signal runs to the vertical direction. Namely the vertical channel is employed. The output of NAND logic is formed on the silicon pillar. This structure is fabricated by using low cost process technology for 3D NAND flash memory [14]-[17, 18].

However, this silicon pillar structure results in the operation of only single logic at the same time within one silicon pillar. Plural number of logic operations within one silicon pillar at the same time can not be realized. Therefore, conventional
Proposal of stacked type Fe-FET ... structure has the problem that the parallel processing within one silicon pillar can not be realized. Parallel processing is the key issue for realizing the high speed operation.

In order to overcome the problem stacked type Fe-FET reconfigurable logic circuit featured with the parallel processing within one silicon pillar has been newly proposed. This novel structure can be realized by using modified process technology of 3D NAND flash memory. For realizing the proposed scheme plural number of logics are generated within one silicon pillar. Furthermore, the outputs of these logics are connected to horizontally running wires and these wires are connected to vertically running wires which act as the output signals. For realizing this structure two improvements for fabrication scheme of 3D NAND flash memory should be introduced. First scheme is various depth trench formation.

Figure 2: Vertically stacked type NAND/NAND array
technology with one fabrication step for silicon pillar of Fe-FET and vertically running wires. Second scheme is connection technology between the output of logic block generated within the silicon pillar to horizontal running wires.

2 Structure of conventional and proposed parallel processing scheme

![Figure 3: Structure of parallel processing scheme.](image-url)

(a) schematic of stacked scheme, (b)(c) conventional scheme, (d)(e) proposed scheme
The structure of conventional and proposed parallel processing scheme is shown in Fig.3. In Fig.3(a) schematics and corresponding circuit is shown. In Fig.3(b)(C) conventional parallel processing scheme are shown. In the conventional scheme only one logic operation can be realized at the same time. Therefore, for realizing the n’th parallel processing n silicon pillar are connected in series as shown in Fig.3(b)(C). If the number of staked layer becomes to large for realizing low fabrication cost Fig.3 (C) is employed in stead of Fig.3(b)[19]. In Fig.3(d)(e) proposed parallel processing scheme are shown. As previously described with the proposed scheme plural logic operations can be successfully realized at the same time. In Fig.3(d) n outputs generated within one silicon pillar are connected vertically running independent wires. For realizing n outputs within one silicon pillar n*k layers structure and independent output structure are introduced. Fig.3(e) shows the improved proposed scheme compared with that of Fig.3(d). In Fig.3(e) the outputs of m adjacent silicon pillars are connected for reducing the number of vertically running wires. This leads to the reduction of pattern area and fabrication process cost.

3 Fabrication process of proposed parallel processing scheme

![Image of fabrication process](image)

Figure 4: Process steps of Fig.3(c), (a) formation of WLs and Dielectric, (b)trench formation, (c)formation of ferroelectric film, (d) formation of P-type silicon,(e)circuit diagram
Figure 5: Process steps of Fig.3(d), (a) formation of WLs, Dielectric and output, (b) trench formation for Fe-FET and vertical output Lines for output1 and output2, (c)formation of ferroelectric film, (d) formation of Dielectric film, (e)formation of n-type diffusion for Fe-FET, (f) formation of P-type silicon, (g)formation of poly silicon for vertical wiring, (h)circuit diagram
For realizing the proposed parallel processing scheme different process technology compared with that of conventional parallel processing scheme should be introduced.

The process steps for conventional parallel processing scheme is shown in Fig.4. Fig.4(a)-(d) shows cross sectional process steps and Fig.4(e) shows corresponding circuit diagram. This process steps are almost the same as that of 3D NAND flash memory.

The process steps of proposed parallel processing scheme corresponding to Fig.3 (d) is shown in Fig.5. As shown in Fig.5(a) not only the WLs and dielectric but also output 1,2 (2 operation case is assumed in this figure) should be stacked. These outputs are formed by the horizontal running wires. After that trenches are formed for realizing vertically running wires and silicon pillar for Fe-FET as shown in Fig.5(b). Trench depths are different as shown in the Figure. For realizing the different trench depths with one step of fabrication process different trench opening size scheme is employed[20][21]. Next ferroelectric film is formed for the silicon pillar as shown in Fig.5(c). After that dielectric is formed for the vertically running wires as shown in Fig.5(d). Next outputs 1,2 and VDD which run for horizontal direction are connected to silicon pillar as shown in Fig.5(e). This process is realized by using thermal diffusion of N+ impurity into P-type silicon from previously stacked N+ rich dielectrics. After that P-type silicon is formed for silicon pillar as shown in Fig.5(f). Finally poly silicon is formed for vertical running wires as shown in Fig.5(g).
For realizing these process novel trench etching process shown in Fig.5(b) is very important. For realizing the different trench depths with one step of fabrication process different trench opening size scheme is employed. It is well known that trench depth caused by the Si etching is strongly depends on the trench opening size. With small trench opening size shallow trench is formed. By using this feature of trench etching and polishing of silicon substrate the process of Fig.5(b) can be successfully realized with only one step of fabrication process as shown in Fig.6. In Fig.6 MEMS process of Ref[20] is assumed.

Next the process steps of proposed parallel processing scheme corresponding to Fig.3 (e) is described. The cross sectional view and corresponding circuit are shown in Fig.7. The process step are almost the same as that of Fig.5. The plural number of silicon pillars are connected in series (4 pillars in Fig.7). Upper part of silicon pillar is used for logics corresponding to signal A and lower part of silicon pillar is used for logics corresponding to signal B. Plural number of adjacent silicon pillar is connected in series. This scheme leads to the small number of vertical running wires compared with that of Fig.5. This feature enable to successfully reduce the pattern area and process cost.

4 Conclusion

In order to realize the parallel processing within one silicon pillar, a novel stacked type Fe-FET reconfigurable logic circuit featured with parallel processing within
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one silicon pillar using modified process technology of 3D NAND flash memory has been newly proposed. For realizing the proposed scheme plural numbers of logics are generated within one silicon pillar. Furthermore, the outputs of these logics are connected to horizontally running wires and these wires are connected to vertically running wires which act as the output signals. For realizing this structure two improvements for fabrication scheme of 3D NAND flash memory should be introduced. First is fabrication process featured by various depth trench formation technology with one fabrication step. Second is connection technology between the output of logic block generated within the silicon pillar to horizontal running wires.

References


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