

High throughput Based Transceiver Design Using Convolutional Encoder and Viterbi Decoder

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Abstract

In digital communication system to reconstruct the data, designs with high throughput is required. Coding and decoding techniques are used in digital communication and satellite communication, to reduce the error rate during the data transmission. Convolutional encoder and Viterbi decoder are used in the proposed system. The Viterbi algorithm is used as the highest throughput design in digital signal processing. The Viterbi decoder is used in high speed implementation due to non-linearity and recursive. This paper will describe the concept of the Viterbi algorithm. The Viterbi algorithm (VA) is mainly employed to decode the convolutional codes. Encoder has less complexity than the decoder. So decoder has to be concentrated more. Viterbi decoder design is simulated using Verilog HDL in Modelsim 6.5b software.

Keywords: Encoder, Viterbi decoding algorithm, BMC, ACS, TBU.

1. Introduction

Convolutional coding and Viterbi decoding are applied to achieve low error rate in communication. In general communication system, signal is transmitted from transmitter to receiver through the channel. During the transmission error rate is drastically reduced while using the convolutional encoder and viterbi decoder. Two major components are encoder and decoder. Convolutional encoder is used here. The

Viterbi algorithm is an effective scheme for decoding the convolutional codes. The output of the encoder directly given as the input to the decoder. Trellis diagram is used to represent the encoder. Output of the decoder can be obtained by applying trace back concept to the trellis diagram. The output of the decoder will be same as the encoder’s input. In this proposed system convolutional encoder with Viterbi decoder in transmitter and receiver has been implemented. [7]

2. Technology description

2.1 Convolutional Encoder

Recursive Convolutional encoder is used in this proposed system [1]. Input is one bit and output will be two bit. Encoder always denoted as (n,k,m).

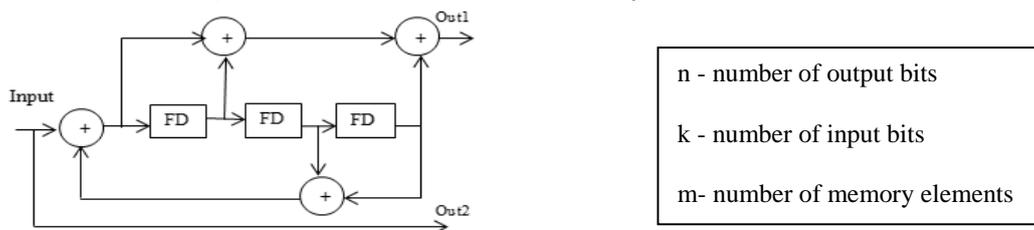


Figure 1: Convolutional encoder

2.2 Viterbi algorithm

Viterbi decoding algorithm was discovered by Viterbi in 1967. The Viterbi algorithm is an efficient method to decode the convolutional codes with maximum-likelihood (ML). Errors can be rectified by this technique even the received data pretended with channel noise. Fixed decoding time is the benefit of the Viterbi algorithm [2]. Trellis diagram representation is the most important section in Viterbi algorithm. It consists of states and branches. Each branch is connected with two states. In this algorithm branch metric has to be calculated first. Next Path metric has to be calculated. To get the decoded output of the trellis diagram, trace back methodology is needed. Path Metric (PM) is needed to represent the paths as $PM_{[i]}(t+1)$ corresponds to state $[i]$ at instant $t+1$. [9]

$$PM_{[i]}(t+1) = \min (PM_{[k]}(t) + BM_{([k][i])(t)}) \longrightarrow \textcircled{1}$$

3. Architecture of Viterbi decoder

The Viterbi decoder has three units. Figure 2 shows the Viterbi decoder’s architecture with three major units. First one is BMU- Branch Metric Unit. The output of the encoder is first given as the input to the BMU. It is used to calculate the

branch metric of each branch. Next unit is the ACS – Add Compare Select unit. This unit is used for calculating path metric and also to select the best one. Next will be the TBU- Trace Back Unit. The decoded output will be obtained in this unit [3].

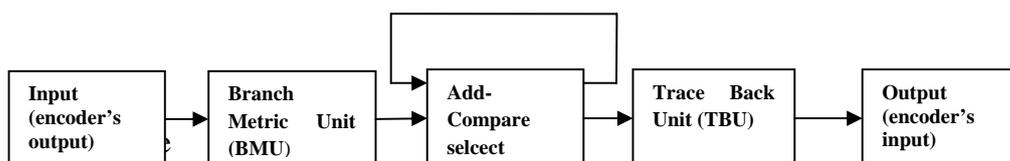


Figure 2: Architecture of Viterbi decoder.

3.1 Branch Metric Unit

Branch Metric Calculation (BMC) modules are used to calculate the difference between the input of the decoder and received input. The encoder trellis diagram starts with the state 000. Decoder also starts with the same state 000. Every state in decoder can be reached from distinct two other states [4]. The BMU computes the branch metric by finding the difference between the probable inputs from the previous states and send to ACS modules for selection. So the BMC computes the two received bits at this instance to the probable inputs (01, 10) and output as a metric. Figure 3 shows the example of Branch metric calculation. [10]

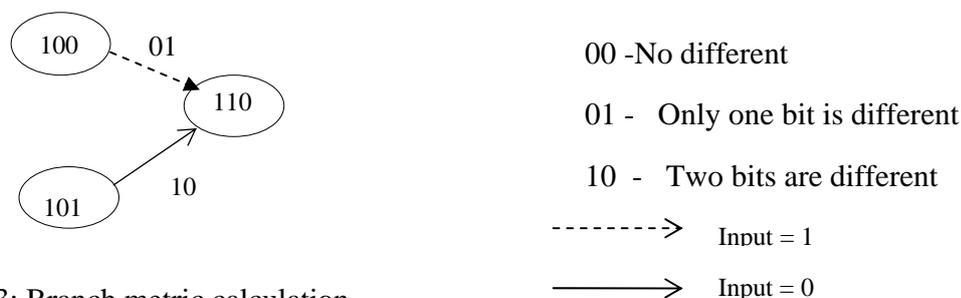


Figure 3: Branch metric calculation

3.2 Add Compare Select Unit

Add Compare Select (ACS) module will add the BMC module’s output to previous path cost of the arriving state. It compares the new path costs of the arriving states and selects the lowest cost path. This path metric will be given to the TBU. The ACS will add all the branch metric of every branch to calculate the path metric. Eight ACS modules are used here [5] [6].

3.3 Trace Back Unit

TBU is used to traverse back in the trellis diagram to determine the decoded output. In this project two TBU are used in parallel. Also four memory banks are used to store the path metric which is received from the ACS. The next state selects the lowest cost predecessor when the trellis mesh builds. At every instance it has only 8 active paths. When trace back methodology applied to trellis the final 8 paths get converged at a point. Correct decoder output will be obtained from that movement. So trace back applied to two memory banks. It can start any point of the final state. It is assumed that one memory bank gets converged the all paths. Then the trace back of the next Memory bank is acceptable. Then it does not need to trace back all 8 paths at the start. It can starts from a random endpoint. It is assured that all end points get converged at an early point in trellis [8]. The selected decode output is written in to display memory.

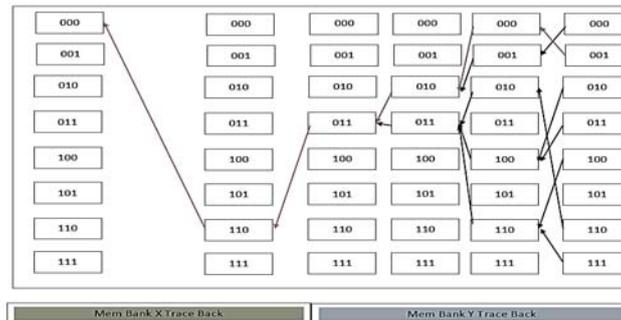


Figure 4: Operation of Trace back module.

4. Result analysis

4.1 Encoder

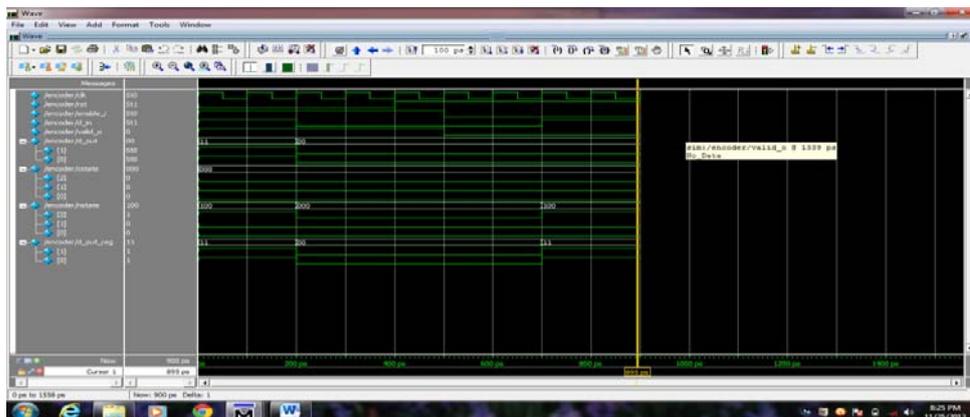


Figure 5: Result of convolutional encoder

5. Conclusion and future work

The transmitter and receiver with encoder and decoder have been implemented. The proposed system has presented, how the Viterbi algorithm plays a pivot role in all kind of communications. Code rate with $\frac{1}{2}$ encoder has been implemented successfully. The functionality of major three units BMC, ACS, TBU has been explained clearly. Among the three units ACS has more complexity than other units. Different architectures are available to implement the ACS to attain low complexity and high performance. The future work will be implemented by using specific architecture in decoder to enhance its performance with different configuration.

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Received: February 1, 2014