Analysis of Bit Cost and Performance for Stacked Type Chain PRAM

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Abstract

The analysis of bit cost and the performance of stacked type chain PRAM has been newly described. Using the optimized number of layer the bit cost of stacked type chain PRAM with stacked horizontal plane structure or BiCS type structure can be reduced compared with that of 1 layer NAND flash memory. The smallest bit cost of BiCS type structure is as small as 0.08 of 1 layer NAND flash memory using the optimized number of layer of 64. The delay time of WL and BL of stacked type chain PRAM with BiCS type structure has been estimated. Using the optimized number layer of 64 for realizing smallest bit cost the delay time of WL and BL are less than 5ns which is competitive to DRAM. Because of estimated high speed characteristics and low bit cost, the chain PRAM with BiCS type structure is the promising candidate for replacing DRAM and NAND flash memory.

Keywords: PRAM, chain structure, PCM, BiCS, bit cost
1 Introduction

PRAM which uses PCM (Phase Change Material) as the data storage has been proposed for the promising candidate of low-cost and high-performance nonvolatile semiconductor memory. At present, the high density PRAM has been developed [1][2]. In the memory cell a transistor and a PCM are connected in series. Recently, chain PRAM has been newly proposed for achieving lower bit cost (fabrication cost of one bit) [3]. It adopts the chain structure [4][5] which connects the parallel connection of a transistor and a PCM connected in series. In [3], this chain structure is fabricated in a horizontal plane (xy plane). We call this as one layer horizontal plane structure. For realizing lower bit cost than one layer horizontal plane structure, stacking of one layer horizontal plane structure [6] (stacked horizontal plane structure) and BiCS (Bit Cost Scalable) type structure [7][8] has been proposed. In this BiCS type structure a chain structure is fabricated in a vertical to the horizontal plane.

In the previous works, the fabrication method [3][7][8] and the memory cell design inherent to the chain structure [7] have been described. However, the analysis of bit cost and the performance (the access time) has not been reported.

In this paper the analysis of bit cost and the performance of stacked type chain PRAM has been newly described. This paper is organized as follows. Section 2 describes the analysis of bit cost of stacked type chain PRAM. Section 3 presents the analysis of access time (delay time of WL and BL). Section 4 describes the configuration of stacked type chain PRAM with 1T bit memory density. Finally, a conclusion of this work is provided in Section 5.

2 Analysis of bit cost of stacked type chain PRAM

Figure 1: Chain PRAM with one layer horizontal plane structure (A) Cross-sectional view, (B) Equivalent circuit
In section 2, bit cost of stacked type chain PRAM has been estimated. Especially the bit cost of two types of stacked type chain PRAM (Fig.2, Fig.3) has been compared analytically.

The cross sectional view of chain PRAM with one layer horizontal plane structure is shown in Fig.1 (A)[3]. The equivalent circuit is shown in Fig.1 (B). As shown in Fig.1 a chain cell structure is fabricated in a horizontal plane. For fabricating this structure 7 process steps should be adopted. That is, ①Formation of SiO₂ under the gate electrode, ②Removal of SiO₂ for the gate electrode formation, ③Fabrication of the gate electrode, ④Fabrication of the gate dielectric, ⑤Fabrication of the silicon for the channel, ⑥Formation of PCM, ⑦Formation of SiO₂ for passivation(Fig.1 (A)). For accessing the selected memory cell the off voltage is applied to the selected memory cell and the on voltage is applied to the pass (unselected) memory cell.

Figure 2: Chain PRAM with stacked horizontal plane structure in the case of N=4, (A) Cross- sectional view, (B)Equivalent circuit

The cross sectional view of chain PRAM with stacked horizontal plane structure is shown in Fig.2 (A)[6]. The equivalent circuit is shown in Fig.2 (B). The stacked horizontal plane structure is fabricated repeating the formation of one layer horizontal plane structure. If the formation of one layer horizontal plane structure is repeated N times, N layers of stacked type chain PRAM can be fabricated. For realizing the N layers of stacked type chain PRAM, 7N process steps are required.
The residual process steps for realizing stacked type chain PRAM, such as formation of the peripheral circuit and wiring, is independent to this 7N process steps. Therefore, if the number of N is large enough, the bit cost with stacked horizontal plane structure can be reduced compared with that with one layer horizontal plane structure.

The cross sectional view of chain PRAM with BiCS type structure is shown in Fig.3 (A)[7]. The equivalent circuit is shown in Fig.3 (B). As shown in Fig.3 a chain cell structure is fabricated in a vertical direction to the horizontal plane. For realizing this structure, the process technology for realizing BiCS type flash memory [9][10] has been introduced. For realizing N layers of stacked type chain PRAM, 2N+5 process steps are required. That is, after the formation N layers of the interlayer dielectric and WLs, ①Trench formation to the SOI substrate, ②Formation of the gate dielectric within the trench, ③Formation of the PCM within the gate dielectric, ④Partial removal of the PCM for realizing the chain structure, and ⑤Formation of silicon for the channel should be introduced. If the number of N is large enough, the process steps 2N+5 is almost equal to 2N. This number of 2N is smaller than 7N of stacked horizontal plane structure case. Therefore the bit cost with BiCS type structure can be reduced compared with that with stacked horizontal plane structure.

Figure 3: Chain PRAM with BiCS type structure in the case of N=4, (A) Cross-sectional view, (B)Equivalent circuit, (C) Top view
By using Fig.2 and Fig.3 the bit cost of stacked type chain PRAM with stacked horizontal plane structure and with BiCS type structure has been compared analytically. In this analysis the bit cost of NAND flash memory with 1 layer is used as a reference. The bit cost of these structures are estimated by using the formula as shown in Fig.4 [11]. When the number of the layer is N, the number of residual process steps for realizing stacked type chain PRAM, such as formation of the peripheral circuit and wiring is assumed to be 50[11]. It is assumed that this number of 50 is independent to the memory cell structure. Almost chip area is occupied by the memory cell in the case of semiconductor memory[12]. Thus, chip area is approximately equal to the area of memory cell. The memory cell area per bit of these structure is 4F^2 (F is feature size). Therefore, using the number of memory cells per one layer, M, chip area of these structures become the same value of M*4F^2. The yield of 1 layer NAND flash memory is assumed to be Y. By using the formula Yield=Y^(number of process steps)/50, the yield of stacked type chain PRAM can be estimated. Chip cost, fabrication cost for 1 bit, is proportional to chip area and the number of process steps, and inversely proportional to the yield. Therefore, using a constant of proportionality, k, chip cost of these structures can be estimated (Fig.4). Bit cost, cost for one bit, is inversely proportional to number of layer. Therefore, the bit cost can be estimated as shown in Fig.4 using a constant of proportionality, L.

<table>
<thead>
<tr>
<th>Number of layer</th>
<th>1 layer type</th>
<th>Stacked horizontal plane structure</th>
<th>BiCS type structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of process steps</td>
<td>50</td>
<td>50+7N</td>
<td>50+2N</td>
</tr>
<tr>
<td>Chip area</td>
<td>M*4F^2</td>
<td>M*4F^2</td>
<td>M*4F^2</td>
</tr>
<tr>
<td>Yield</td>
<td>Y</td>
<td>Y^(50+7N)/50</td>
<td>Y^(50+2N)/50</td>
</tr>
<tr>
<td>Chip cost</td>
<td>k<em>M</em>4F^2*50)/Y</td>
<td>k<em>M</em>4F^2*50 + (50+7N))/Y^(50+7N)/50</td>
<td>k<em>M</em>4F^2*50 + (2N))/Y^(50+2N)/50</td>
</tr>
<tr>
<td>Bit cost</td>
<td>L<em>M</em>4F^2<em>50)/(N</em>Y)</td>
<td>L<em>M</em>4F^2<em>50 + (50+7N))/N</em>Y^(50+7N)/50</td>
<td>L<em>M</em>4F^2<em>50 + (50+2N))/N</em>Y^(50+2N)/50</td>
</tr>
</tbody>
</table>

Figure 4: The estimation of bit cost of stacked type chain PRAM

Estimated bit cost of stacked type chain PRAM vs number of layer is shown in Fig.5. The yield of 1 layer NAND flash memory, Y, is used as a parameter (Y=70%,90%,95%). In all cases, at first, the bit cost decreases with increasing the number of layer, and after that increases with increasing the number of layer. This is because, at first, the bit cost decreases with increasing number of layer, and after that the bit cost increases with decreasing yield. This feature is enhanced.
with decreasing $Y$. As a result, there is the optimized number of layer where the bit cost becomes minimum value (arrow in Fig.5). In the same $Y$ case, the minimum bit cost of BiCS type structure is smaller (about 30%) than that of stacked horizontal plane structure. This is because, the required process steps per layer of BiCS type structure, $2N$, is smaller than that of stacked horizontal plane structure, $7N$. In Fig.5 bit cost of 1 indicates the bit cost of 1 layer NAND flash.

**Figure 5:** Bit cost of stacked type chain PRAM vs number of Layer

**Figure 6:** Optimized number of layer for stacked type chain PRAM
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memory as a reference. The bit cost of 1 layer NAND flash memory is smallest among the presently available semiconductor memory. Fig.5 shows that in the case of Y=90%, the smallest bit cost of BiCS type structure is as small as 0.08 compared with that of 1 layer NAND flash memory using the optimized number of layer of 64. This result indicates that because of low bit cost stacked type chain PRAM with BiCS type structure is the promising candidate for replacing the 1 layer NAND flash memory. Of course, the smallest bit cost of stacked horizontal plane structure of 0.28 is also available for realizing low cost semiconductor memory. Fig.6 shows the optimized number of layer for stacked type chain PRAM as a function of number of process steps/layer. In this figure 2 of number of process steps/layer indicates BiCS type structure and 7 indicates stacked horizontal plane structure. As increasing the number of process steps/layer the minimum bit cost increases and the optimized number of layer decreased. Smaller bit cost is realized with large Y, small number process steps/layer and large optimized number of layer.

3 Analysis of access time of stacked type chain PRAM

As described in section 2, in the same Y case, the minimum bit cost of BiCS type structure is smaller (about 30%) than that of stacked horizontal plane structure. Therefore, only the access time of BiCS type structure has been estimated in this section. Firstly, it is estimated that whether the access time of BiCS type structure is competitive to DRAM which features with high speed operation or not. To realize high speed operation competitive DRAM, delay time of WL and delay time of BL should be limited to smaller than 10% of DRAM access time of 50ns (5ns)[13].

Figure 7: The view of memory cell, (A)Top view, (B)Cross sectional view
For estimating the resistance and capacitance of WL and BL, the top view and cross-sectional view of memory cell is used. The view of memory cell is shown in Fig.7 ((A)Top view, (B)Cross sectional view). F=39nm is employed for this estimation[11][13]. Channel width is 2F (shown by the circles in Fig.7(A)).

The resistance of WL per cell is 0.61Ω using the pattern of WL shown in Fig.7 (A) and sheet resistance of 0.1Ω/□. WL capacitance per cell is 0.315fF. As a result the delay time of WL which can be estimated 1.26pF*2.44KΩ becomes 3.07ns, if 4K memory cells are connected to one WL. If 8K memory cells are connected one WL, the delay time exceeds upper limit of 5ns.

![Figure 8: Total resistance of BL](image1)

![Figure 9: Cross sectional view of memory cell about total capacitance of BL](image2)

The figure for estimating the total resistance of BL is shown in Fig.8. It is assumed that N layer (N stage) of memory cell is employed. In the case of chain structure there is a relationship between the resistance of pass transistor RP and the resistance of PCM RL. For realizing stable read write operation RP / RL should be smaller than 0.46 [7]. And also, RP must be small enough for realizing high speed operation. The minimum value of RP is about 1.2KΩ in the case of 32-50nm design rule[7]. As a result, the total of resistance of BL becomes 1.2 KΩ *(N-1)+2.6 KΩ. When N=64, the total of resistance of BL becomes 78.2KΩ.

The figure for estimating the total capacitance of BL is shown in Fig.9. The capacitance of BL is consisted with gate capacitance of pass transistor and selected transistor. The total capacitance of BL becomes N*(gate capacitance per
memory cell). When N=64, the total of capacitance of BL becomes 0.020pF. As a result, the delay time of BL becomes 78.2KΩ*0.020pF=1.56ns. If N=128 is employed, the delay time of BL excesses upper limit of 5ns. From the estimation of delay time of BL, for realizing the high speed operation competitive to DRAM the number of stacked layer N is limited to 64. As described in Section 2, optimized number of layer for realizing the minimum bit cost is about 32-128. Therefore, by using N=64, both high speed operation competitive to DRAM and lowest bit cost of 0.08 compared with 1 layer NAND flash memory can be successfully achieved.

4 Configuration of 1T bit stacked type chain PRAM

Using the estimation in Section 2 and 3, configuration of 1T bit stacked type chain PRAM has been investigated (Fig.10). Stacked type chain PRAM has both high speed characteristic competitive to DRAM and lower bit cost than 1 layer NAND flash memory. As a result, this chip can replaces 32G bit DRAM and 992G bit NAND flash memory as shown in Fig.10. 1T bit chip is consisted with 1024 1G bit memory blocks. For realizing high speed performance and low bit cost 1G bit memory block has 64 layer structure. 4K memory cells are connected to one WL. For realizing the high speed operation 32G bit for DRAM replace is located near the peripheral circuit which controls the memory blocks. For realizing lower bit cost 992G bit for replace NAND flash memory is located near and far from the peripheral circuit.
By using this 1T bit stacked type chain PRAM the conventional memory hierarchy with DRAM and flash memory[14] can be replaced to new memory hierarchy with stacked type chain PRAM. Newly proposed memory hierarchy is shown in Fig.11.

![Figure 11: Newly proposed memory hierarchy](image)

### 5 Conclusion

The analysis of bit cost and the performance of stacked type chain PRAM has been newly described. Using the optimized number of layer the bit cost of stacked type chain PRAM with stacked horizontal plane structure or BiCS type structure can be reduced compared with that of 1 layer NAND flash memory. The smallest bit cost of BiCS type structure is as small as 0.08 of 1 layer NAND flash memory using the optimized number of layer of 64 (Y=90%). The delay time of WL and BL of stacked type chain PRAM with BiCS type structure has been estimated. Using the optimized number layer of 64 for realizing smallest bit cost the delay time of WL and BL are less than 5ns which is competitive to DRAM. Because of estimated high speed characteristics and low bit cost, the chain PRAM with BiCS type structure is the promising candidate for replacing DRAM and NAND flash memory.

### References


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